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LM32019CFW-1

LCD Module User Manual

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Rev.	Descriptions	Release Date
0.1	New release	2008-09-03
0.2	Update Backlight Characteristics	2009-06-12

Table of Content

1. Basic Specifications

1.1 Display Specifications

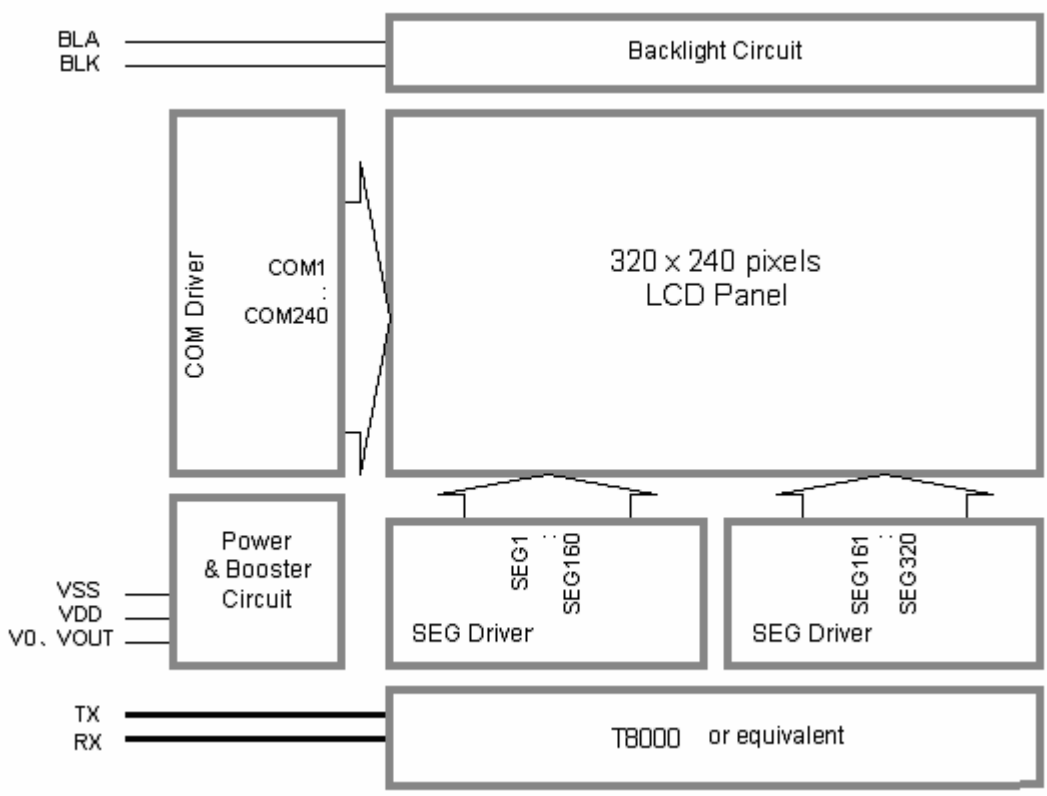
1) LCD Display Mode : STN, Negative, Transmissive
2) Display Color : Display Data = “1” : Light Gray (*1)
: Display Data = “0” : Dark Blue (*2)
3) Viewing Angle : 12 H
4) Driving Method : 1/240 duty, 1/14 bias
5) Backlight : White LED backlight

Note:
*1. Color tone may slightly change by Temperature and Driving Condition.
*2. The Color is defined as the inactive / background color

1.2 Mechanical Specifications

1) Outline Dimension : 159.0 x 107.8 x 11.0 MAX.
see attached Outline Drawing for details

1.3 Block Diagram



1.4 Terminal Functions

Pin No.	Pin Name	I/O	Descriptions
1	TX	output	Data Transmits Signal
2	RX	input	Data Receive Signal
3	VSS	power	0V Power Supply, GND
4	VDD	power	Positive Power Supply
5	V0	input	LCD Contrast Reference Input
6	VOUT	output	Power Booster Output for V0
7	BLA	power	Backlight positive power
8	BLA	power	Backlight positive power
9	BLK	power	Backlight negtive power
10	BLK	power	Backlight negtive power

2. Absolute Maximum Ratings

Items	Symbol	Min.	Max.	Unit	Condition
Supply Voltage	V_{DD}	-0.3	+5.5	V	V_{SS} = 0V
Input Voltage	V_{RX}	-6.5	+6.5	V	V_{SS} = 0V
Operating Temperature	T_{OP}	-20	+70	°C	No Condensation
Storage Temperature	T_{ST}	-30	+80	°C	No Condensation

Cautions:
Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

3. Electrical Characteristics

3.1 DC Characteristics

V_{SS}=0V, V_{DD}=5.0V, T_{OP}=25°C

Items	Symbol	MIN.	TYP.	MAX.	Unit	Applicable Pin
Operating Voltage	V_{DD}	4.5	5.0	5.5	V	VDD
Input High Voltage (*1)	V_{INH}	+2.4	-	+6.5	V	RX
Input Low Voltage (*1)	V_{INL}	-6.5	-	-0.8	V	RX
Output High Voltage (*1)	V_{OUTH}	+5.0	+5.4	-	V	TX
Output Low Voltage (*1)	V_{OUTL}	-	-5.4	-5.0	V	TX
LCD Contrast Reference Voltage (*2)	V_0	-	22.9	-	V	V0
Frame Freq.	f_{FRAME}	60	66	80	Hz	
Operating Current	I_{DD}	-	50	-	mA	VDD

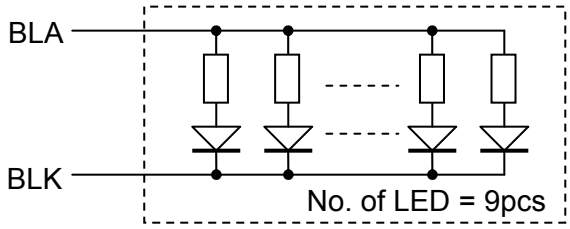
Note: *1. Please refer to MAX3232 datasheet for details.
*2. Frame freq. at 66Hz

3.2 LED Backlight Circuit Characteristics

BLK=0V, If_{BLA}=153mA, T_{OP} =25°C

Items	Symbol	MIN.	TYP.	MAX.	Unit	Applicable Pin
Forward Voltage	Vf_{BLA}	-	5.0	-	V	BLA
Forward Current	If_{BLA}	-	153	200	mA	BLA

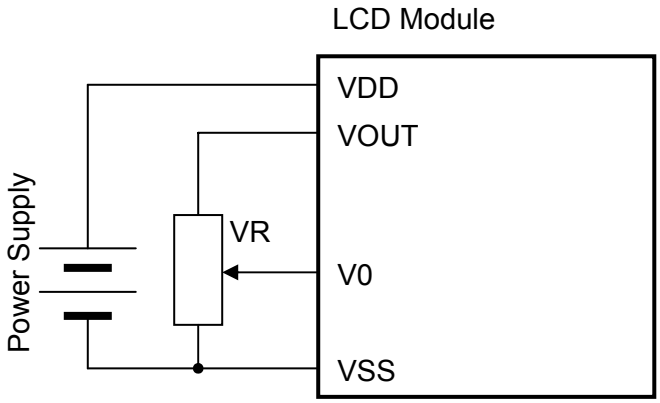
Cautions:
Exceeding the recommended driving current could cause substantial damage to the backlight and shorten its lifetime.



4. Function Specifications

4.1 Adjusting the Display Contrast

A Variable-Resistor must be connected to the LCD module for providing a reference to V0. Adjusting the VR will result the change of LCD display contrast.
The recommended value of VR is 25k to 50k



4.2 UART Serial Host Communication Packet Format

In UART serial host mode, each communication packet starts with a byte of “FF” and ended with “FE”. Length of parameters (one byte) is also required into the packet. An Acknowledge Packet will be sent back to the UART serial host by the T8000 once the command is finished execution.

UART Serial host Communication Packet Format

Sequence	No of byte	Content
1	1	0xFF (hex) <START BYTE>
2	1	Opcode
3	1	Length of Parameters
4	1 to 64	Parameters / Data (up to 64bytes)
5	1	0xFE (hex) <END BYTE>

Note: A “FF” bytes sequence of length equal to or more than 65 will cause re-synchronization.

UART Serial host re-synchronization Packet Format

Sequence	No of byte	Content
1	Equal or more than 65	0xFF (hex)
2		0xFF (hex)
:		:
:		:

Note: A “FF” bytes sequence of length equal to or more than 65 will cause re-synchronization.

For commands required read data (Opcode 82) from the T8000, it will send read data embedded in the Acknowledge Packet automatically when data is ready.

UART Serial host Acknowledge Packet Format, without “register read data”

Sequence	No of byte	Content
1	1	0x00 (hex)

UART Serial host Acknowledge Packet Format, with “register read data”

Sequence	No of byte	Content
1	1	Register read data
2	1	0x00 (hex)

4.3 Opcode Descriptions

Opcode (hex)	Operations	No of Parameters / Data (byte)	Parameters / Data
00	Set "Control & Status Port" of the Command Interpreter	1	The value of this data will be directly written to the Control & Status register.
10	charset_config	1	00: Built in 8x8 ASCII 01: 8x8 CGRAM (Embedded RAM) 02: 8x16 CGRAM (Embedded RAM) 03: 16x16 CGRAM (Embedded RAM) 04: 16x16 GB2312-80 (External ROM) 05: 16x16 BIG5 (External ROM) 06: 8x8 Custom 8-bit encoding (External ROM) 07: 8x8 Custom 16-bit encoding (External ROM)
12	set_print_coord	4	Character Print Coordinates x-coordinate (2-bytes) y-coordinate (2-bytes) * Mono LCD, x = (multiple of 8) – 1 * Color LCD, no restriction on the value of x coordinate
14	set_font_fgcolor	2	Character Foreground Color (same as td_fgcolor) * Mono LCD: 1bpp, 2bpp, 4bpp * Color LCD: 12-bit STN (4R:4G:4B)
15	set_font_bgcolor	2	Character Background Color * LCD: 1bpp, 2bpp, 4bpp * LCD: 12-bit STN (4R:4G:4B)
16	show_char	1 or 2	Display Character
17	show_string	1 + (1 to 63)	Display String No. of characters (1-byte) Character String (1 to 63-bytes)
19	define_CGRAM	1 + (1 to 32)	CGRAM Bitmap Character code (1 byte) Bitmap pattern (1 to 32 bytes)
20	td_fgcolor	2	Set Foreground Color *Mono LCD: 1bpp, 2bpp, 4bpp *Color LCD: 12-bit STN (4R:4G:4B)
23	draw_pixel	4	Draw Pixel x-coordinate (2-bytes) y-coordinate (2-bytes)
24	draw_line	8	Draw Line x_start (2-bytes) y_start (2-bytes) x_end (2-bytes) y_end (2-bytes)
26	draw_rect	8	Draw Hollow Rectangle (Box) x_start (2-bytes) y_start (2-bytes) x_end (2-bytes) y_end (2-bytes)
27	fill_rect	8	Fill Rectangle (Box) x_start (2-bytes) y_start (2-bytes) x_end (2-bytes) y_end (2-bytes)
28	draw_circle	5	Draw Circle x_center (2-bytes) y_center (2-bytes) radius (1-byte)
29	fill_circle	5	Fill Circle x_center (2-bytes) y_center (2-bytes) radius (1-byte)
60	set_baud	2	Set baud rate divisor (lower byte) divisor (upper byte)
80	refresh_setting	0	-
81	set_mem_ptr	3	Set memory pointer address (3-bytes)
82	read_reg	2	Read register(*ONLY used in UART serial host mode) address (2 bytes)
83	write_reg	2 + 1	Write register address (2-bytes) data (1-byte)
84	write_mem	1 + (1 to 63)	Write memory No. of data (1 byte) data (1 to 63 bytes)
8F	clk_en	6	Enable memory clock; [69, 45, 61, 67, 6C, 65 (6-bytes in hex)]

4.4 System Configuration Registers

Address (hex) A15 ~ A0	R/W	Reset Value	Descriptions
F000	Read / Write	1000 0000	Chip ID Port, Always read back 80 (hex) for T8000 Write "DE FC 0B" (hex) to enable memory clock, same as command with OPCODE "8F".
F001	Read	0000 0000	Chip Revision Port, Always read back 00 (hex) for T8000
F004	Write	-	Command Packet Port - Writing of Command Packets.
F006	Write	xxx1 xxx0	Port for writing control or reading status Bit[7:4] : Reserved Bit[3] : DISPLAY ON / OFF 0=DISPLAY ON 1=DISPLAY OFF Bit[2:1] : Reserved Bit[0] : End of Command, Write "1" after each command packet
	Read	xxxx xxx0	Bit[7:1] : Reserved Bit[0] : FIFO full Read "1" if Command FIFO is full. Hosts must read this bit = "0" before writing to Command Packet Port.
F080	Read / Write	0000 0000	Bit[7:4] : Reserved Bit[3] : STN Panel I/F Data Width 0=4-bit single 1=8-bit single Bit[2] : Color Mode Select 0=Monochrome 1=Color Bit[1:0] : Color Depth Select If Monochrome (Bit[2]=0) 00=1 bit-per-pixel 01=2 bit-per-pixel 10=4 bit-per-pixel 11=Reserved If Color (Bit[2] = 1) 01=12 bit-per-pixel (CSTN panel) 00=Reserved 10=Reserved 11=Reserved
F081	Read / Write	x000 0000	Bit[7] : Reserved Bit[6:0] : Panel Horizontal Character Count – 1, Panel Horizontal Character Count[8:0] supports horizontal panel size up to 128 characters or 1024 pixels.
F082	Read / Write	0000 0000	Bit[7:0] : Panel Line Count - 1 bit[7:0]
F083	Read / Write	xxxx xxx0	Bit[7:1] : Reserved Bit[0] : Panel Line Count – 1 bit[8], Panel Line Count[8:0] supports vertical panel size up to 512 lines.
F084	Read / Write	0000 0000	Bit[7:0] : Display Start Position X Coordinate – bit[7:0]
F085	Read / Write	xxxx xx00	Bit[7:2] : Reserved Bit[1:0] : Display Start Position X Coordinate – bit[9:8]
F086	Read / Write	0000 0000	Bit[7:0] : Display Start Position Y Coordinate – bit[7:0]
F087	Read / Write	xxxx xx00	Bit[7:2] : Reserved Bit[1:0] : Display Start Position Y Coordinate – bit[9:8]
F088	Read / Write	0000 0000	LCD_LUT1 Bit[7:4] : for Gray level 3 Bit[3:0] : for Gray level 2
F089	Read / Write	0000 0000	LCD_LUT0 Bit[7:4] : for Gray level 1 Bit[3:0] : for Gray level 0
F08A	Read / Write	x000 0000	Bit[7] : Reserved Bit[6:0] : Virtual Display Character count – 1 It supports horizontal virtual size up to 128 characters or 1024 pixels.
F08B	Read / Write	xx00 0000	Bit[7:6] : Reserved Bit[5:0] : WF count for STN panels 000000=WF pin toggles every frame 000001=WF pin toggles every 2 LP pulses 000010=WF pin toggles every 3 LP pulses : 111111=WF pin toggles every 64 LP pulses
F08C	Read / Write	xxxx 0000	Bit[7:4] : Reserved Bit[3:0] : Horizontal non-display period 0000=2 characters (16 pixels) 0001=3 characters (24 pixels) : 1111=17 characters (136 pixels)

F08D	Read / Write	xxxx 0000	Bit[7:4] : Reserved Bit[3:0] : Vertical non-display period 0000: 1 line 0001: 2 lines : 1111: 16 lines
F08E	Read / Write	0000 000x	Bit[7:4] : Pixel Clock Divider 0000=24 MHz (divided by 1) 0001=12 MHz (divided by 2) 0010=8 MHz (divided by 3) 0011=6MHz (divided by 4) : 1111=1.5MHz (divided by 16) Bit[3] : Display Blank 0=Normal 1=Blank Bit[2] : Display Invert 0=Normal 1=Invert Bit[1] : LCD_ON Polarity 0=LCD_ON pin active low 1=LCD_ON pin active high Bit[0] : Reserved
F08F	Read /Write	x000 0000	Bit[7] : Reserved Bit[6:0] : Number of frames to start – 1 (Maximum 128 frames)
F090	Read /Write	xx00 0000	Bit[7:6] : Reserved Bit[5:0] : Horizontal Front Porch for TFT panels 000000=1 pixel 000001=2 pixels : 111111=64 pixels
F091	Read /Write	xx00 0000	Bit[7:6] : Reserved Bit[5:0] : Horizontal Back Porch for TFT panels 000000=1 pixel 000001=2 pixels : 111111=64 pixels
F092	Read /Write	xxx0 0000	Bit[7:5] : Reserved Bit[4:0] : Horizontal Pulse Width for TFT panels 00000=1 pixel 00001=2 pixels : 11111=32 pixels
F093	Read /Write	0000 0000	Bit[7:0] : Scratch Pad register
F094	Read /Write	xx00 0000	Bit[7:6] : Reserved Bit[5:0] : Vertical Front Porch for TFT panels 000000=1 line 000001=2 lines : 111111=64 lines
F095	Read /Write	xx00 0000	Bit[7:6] : Reserved Bit[5:0] : Vertical Back Porch for TFT panels 000000: 1 line 000001: 2 lines : 111111: 64 lines
F096	Read /Write	xxx0 0000	Bit[7:5] : Reserved Bit[4:0] : Vertical Pulse Width for TFT panels 00000: 1 line 00001: 2 lines : 11111: 32 lines
F100	Read /Write	00xx xx00	Bit[7] : Enable / Disable 0=Disable Sprite 1=Enable Sprite Bit[6] : Transparency 0=Transparency disable 1=Transparency enable When enabled: Sprite data = 00 becomes transparent and LCD background will be displayed instead. Bit[5:2] : Reserved Bit[1:0] : Sprite Modes Select 00=reserved 01=Sprite with 2 bit-per-pixel 10=reserved 11=reserved
F102	Read /Write	0000 0000	Bit[7:0] : SP_LUT0L[7:0]
F103	Read / Write	0000 0000	Bit[7:0] : SP_LUT0H[7:0]
F104	Read / Write	0000 0000	Bit[7:0] : SP_LUT1L[7:0]

F105	Read / Write	0000 0000	Bit[7:0] : SP_LUT1H[7:0]
F106	Read / Write	0000 0000	Bit[7:0] : SP_LUT2L[7:0]
F107	Read / Write	0000 0000	Bit[7:0] : SP_LUT2H[7:0]
F108	Read / Write	0000 0000	Bit[7:0] : SP_LUT3L[7:0]
F109	Read / Write	0000 0000	Bit[7:0] : SP_LUT3H[7:0]
F10A	Read / Write	0000 0000	Bit[7:0] : Sprite Horizontal Pixel Count – 1 Maximum 256 pixels
F10B	Read / Write	0000 0000	Bit[7:0] : Sprite Vertical Line Count – 1 Maximum 256 lines
F10C	Read / Write	0000 0000	Bit[7:0] : Sprite Horizontal Start Position bit[7:0]
F10D	Read / Write	xxxx xx00	Bit[7:2] : Reserved Bit[1:0] : Sprite Horizontal Start Position bit[9:8] Sprite Horizontal Start Position bit[9:0] is measured in pixels and counted from left to right of the edge of the panel display (i.e. not virtual display).
F10E	Read / Write	0000 0000	Bit[7:0] : Sprite Vertical Start Position bit[7:0]
F10F	Read / Write	xxxx xxx0	Bit[7:1] : Reserved Bit[0] : Sprite Vertical Start Position bit[8] Sprite Vertical Start Position bit[8:0] is measured in lines and counted from top to bottom of the edge of the panel display (i.e. not virtual display).
F142	Write Only	0000 0000	Bit[7:0] : Sprite / overlay storage starting address bit[7:0]
F143	Write Only	0000 0000	Bit[7:0] : Sprite / overlay storage starting address bit[15:8]
F144	Write Only	0000 0000	Bit[7:2] : Reserved Bit[1:0] Sprite / overlay storage starting address bit[17:16] This is the starting address to put the sprite/overlay image
F180	Read Only	0000 0000	Bit[7:0] : Background Color bit[7:0]
F181	Read Only	0000 0000	Bit[7:0] : Background Color bit[15:8]
F182	Read Only	0000 0000	Bit[7:0] : Foreground Color bit[7:0]
F183	Read Only	0000 0000	Bit[7:0] : Foreground Color bit[15:8]
F500	Read / Write	1110 1110	CS0 Configuration Port - Pulse Width Bit[7:4] : Write Cycle Pulse Width 0000=1 memory clock (24 MHz -> 41.6ns) 0001=2 memory clocks : 1110=15 memory clocks 1111=Reserved Bit[3:0] : Read Cycle Pulse Width 0000=1 memory clock (24 MHz -> 41.6ns) 0001: 2 memory clocks : 1110:15 memory clocks 1111: Reserved
F501	Read / Write	0000 0000	CS0 Configuration Port - Control Bit[7] : Enable bit 0=Disable CS0 1=Enable CS0 Bit[6] : Memory data bus width 0=8-bit memory data bus width 1=16-bit memory data bus width Bit[5] : 16-bit SRAM option 0=two 8-bit SRAMs 1=one 16-bit SRAM Bit[4] : Reserved Bit[3] : CS0 assertion time relative to address assertion. 0=CS0 and address assert at the same time 1=CS0 lags address by 1 memory clock. Bit[2] : CS0 Negation Timing 0=CS0 and Address negate at the same time 1=CS0 leads Address by 1 memory clock in write access. Bit[1] : Write Enable Assertion Time 0=Write Enable and Address Assert at the same time. 1=Write Enable lags Address by 1 memory clock. Bit[0] : Write Enable Negation Time 0=Write Enable and Address negate at the same time. 1=Write Enable leads Address by 1 memory clock.

F504	Read / Write	Bit[3:0] = 1110	CS1 Configuration Port - Pulse Width Bit[7:4] : Reserved Bit[3:0] : Read Cycle Pulse Width 0000=1 memory clock (24 MHz -> 41.6ns) 0001=2 memory clocks 0001=3 memory clocks : 1101=14 memory clocks 1110=15 memory clocks 1111=Reserved
F505	Read / Write	0000 0000	CS1 Configuration Port - Control Bit[7] : Enable bit 0=Disable CS1 1=Enable CS1 Bit[6] : Memory data bus width 0=8-bit memory data bus width 1=16-bit memory data bus width Bit[5] : Reserved Bit[4] : Reserved Bit[3] : CS1 assertion time relative to address assertion. 0=CS1 and Address assert at the same time 1=CS1 lags Address by 1 memory clock. Bit[2] : CS1 Negation Timing 0=CS1 and Address negate at the same time 1=CS1 leads Address by 1 memory clock in write access. Bit[1:0] : Reserved
F6C4	Read / Write	xx11 0011	Set Memory Clock Divide Bit[7:6] = Reserved Bit[5:0] = 010000 to set 24MHz memory clock for proper operations

4.5 UART Serial Driving program (Example)

```
// MPU is 89S52 and system clock is 11.0592MHz)
//   subprogram of send a command
void SdCmd(uchar Command)
{
 SBUF = Command;
 while(TI==0)
 {}
 TI=0;
}
// subprogram of send end code
void CmdEnd()
{
 SBUF = 0xfe;
 while(TI==0)
 {}
 TI=0;
}
// subprogram of a command package
void WritePKG(uchar *pkg)
{
    uchar i;
    i=*pkg;
        SdCmd(0xff);
    SdCmd(*(++pkg));
    i=i-1;
        SdCmd(i);
    for(i;i>0;i--)
        SdCmd(*(++pkg));
    CmdEnd();
    delayms(10);
}

// subprogram of initial module

//-----------------------ROM SET-------------------------------
uchar code Set_F504[]={4,0x83,0x04,0xf5,0x04};         // first number is written data number
uchar code Set_F505[]={4,0x83,0x05,0xf5,0x80};
uchar code Set_F6C4[]={4,0x83,0xc4,0xf6,0x10};
//-----------------------STN SET---------------------------------
uchar code Set_F08E[]={4,0x83,0x8e,0xf0,0x22};
uchar code Set_F088[]={4,0x83,0x88,0xf0,0x50};
uchar code Set_F089[]={4,0x83,0x89,0xf0,0xfa};
//----------------------CLOCK SET-----------------------------
uchar code Set_8F[]={7,0x8f,0x69,0x45,0x61,0x67,0x6c,0x65};
//-------------------------------------------------------------
void initLCDM(void)
{
   uchar i;
//   reset module
    PCON=0x00;          // smod=0
    SCON=0x50;
    TCON=0x40;
    TL1=0x00;
    TH1=0x00;          // min bps
    TMOD=0x22;
    for(i=0;i<10;i++)
      {
       SBUF = 0x00;   // reset=0
       while(TI==0)
       {}
       TI=0;
      }
   delayms(100);

// set 9600 bps base on MPU's clock is 11.0592MHz
   PCON=0x00;     // smod=0;
   SCON=0x50;     //mode 1, received,  8N1
   TH1=0xfd;          //  set 9600bps
   TCON=0X40;     // timer 1 operate
   TMOD=0x22;    //  timer 1,mode 2 auto reload
    WritePKG(Set_F504);
    WritePKG(Set_F505);
    WritePKG(Set_F6C4);
    WritePKG(Set_F08E);
    WritePKG(Set_F088);
    WritePKG(Set_F089);
WritePKG(Set_8F);

SdCmd(0xff);        // display on
SdCmd(0x00);
SdCmd(0x00);
CmdEnd();
}
```

5. Design and Handling Precaution

1. The LCD panel is made by glass. Any mechanical shock (eg. dropping form high place) will damage the LCD module.
2. Do not add excessive force on the surface of the display, which may cause the Display color change abnormally.
3. The polarizer on the LCD is easily get scratched. If possible, do not remove the LCD protective film until the last step of installation.
4. Never attempt to disassemble or rework the LCD module.
5. Only Clean the LCD with Isopropyl Alcohol or Ethyl Alcohol. Other solvents (eg. water) may damage the LCD.
6. When mounting the LCD module, make sure that it is free form twisting, warping and distortion.
7. Ensure to provide enough space (with cushion) between case and LCD panel to prevent external force adding on it, or it may cause damage to the LCD or degrade the display result.
8. Only hold the LCD module by its side. Never hold LCD module by add force on the heat seal or TAB.
9. Never add force to component of the LCD module. It may cause invisible damage or degrade of the reliability.
10. LCD module could be easily damaged by static electricity. Be careful to maintain an optimum anti-static work environment to protect the LCD module.
11. When peeling off the protective film from LCD, static charge may cause abnormal display pattern. It is normal and will resume to normal in a short while.
12. Take care and prevent get hurt by the LCD panel sharp edge.
13. Never operate the LCD module exceed the absolute maximum ratings.
14. Keep the signal line as short as possible to prevent noisy signal applying to LCD module.
15. Never apply signal to the LCD module without power supply.
16. IC chip (eg. TAB or COG) is sensitive to the light. Strong lighting environment could possibly cause malfunction. Light sealing structure casing is recommend.
17. LCD module reliability may be reduced by temperature shock.
18. When storing the LCD module, avoid exposure to the direct sunlight, high humidity, high temperature or low temperature. They may damage or degrade the LCD module