



Connecting EPSON Display Controllers to Topway LCD Panels

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1 Introduction

This document provides connection information enabling EPSON Display Controllers to control a variety of Shenzhen TOPWAY Technology CO.,LTD LCD panels. This document includes connector details, pin mappings, and example register settings.

For detailed technical information on EPSON Display Controllers or Shenzhen TOPWAY LCD panels, please refer to the specification or technical manual for each product.

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2 Display Controller Compatibility

This document discusses the following Shenzhen Topway TFT panel.

- LMT035KDH03 (a-Si TFT, 3.5inch, 320x240)

The Shenzhen Topway TFT panel is compatible with one or more of the following EPSON display controllers.

- S1D13781 (QFP 100-pin)

For further information on the Topway TFT panel go to the Shenzhen TOPWAY Technology CO.,LTD LCD products web site <http://www.topwaydisplay.com/Product/LCDM-Color/index.htm>

3 Connecting to the LMT035KDH03

The LMT035KDH03 TFT panel is compatible with the S1D13781 display controller. The following sections will provide connector details, pin mappings, and example register settings for these combinations.

3.1 LMT035KDH03 Pin Mapping

The LMT035KDH03 TFT panel uses a 54-pin connector with the following pin mapping.

Table 3-1 LMT035KDH03 Pin Mapping

Connector Pin#	Pin Name	Pin Description
1	LED_CATHODE	Backlight LED CATHODE Supply
2	LED_CATHODE	Backlight LED CATHODE Supply
3	LED_ANODE	Backlight LED ANODE Supply
4	LED_ANODE	Backlight LED ANODE Supply
5	NC	No Connection
6	NC	No Connection
7	NC	No Connection
8	/RES	Hardware Reset
9	/SPEN	SPI enable signal, active LOW, normal HIGH
10	SPCK	SPI clock signal, rising edge trigger
11	SPDA	SPI Data signal
12	D0	Blue data0
13	D1	Blue data1
14	D2	Blue data2
15	D3	Blue data3
16	D4	Blue data4
17	D5	Blue data5
18	D6	Blue data6
19	D7	Blue data7
20	D8	Green data0
21	D9	Green data1
22	D10	Green data2
23	D11	Green data3
24	D12	Green data4
25	D13	Green data5
26	D14	Green data6
27	D15	Green data7
28	D16	Red data0
29	D17	Red data1
30	D18	Red data2
31	D19	Red data3

Connector Pin#	Pin Name	Pin Description
32	D20	Red data4
33	D21	Red data5
34	D22	Red data6
35	D23	Red data7
36	HSYNC	Horizontal Sync Signal
37	VSYNC	Vertical Sync Signal
38	DCLK	Data Clock input
39	NC	No Connection
40	NC	No Connection
41	VDD	Positive Power Supply
42	VDD	Positive Power Supply
43	NC	No Connection
44	NC	No Connection
45	NC	No Connection
46	NC	No Connection
47	NC	No Connection
48	NC	No Connection
49	NC	No Connection
50	NC	No Connection
51	NC	No Connection
52	DEN	Data Enable input
53	GND	Power Ground Supply
54	GND	Power Ground Supply

Note

The recommended connector is a FH28-54S-0.5SH from Hirose Electric Co., Ltd. The connector is a 0.5mm pitch 54-pin FPC connector (2.55mm thickness).

3.2 Connection Examples

The information in this section provides connection examples for the S1D13781 display controllers. In addition to the pin connections for the selected display controller, the LMT035KDH03 requires the following power supplies.

VDD +3.3V typical (3.0 - 3.3V)

VfBLA +20.0V typical

For VCC, select a voltage within the supportable range of the Display Controller.

For further details on the LMT035KDH03, such as power consumption and absolute maximum ratings, please contact your Shenzhen TOPWAY representative.

3.2.1 Connecting the LMT035KDH03 to the S1D13781

The following diagram shows an example implementation of the LMT035KDH03 panel connected to the S1D13781.

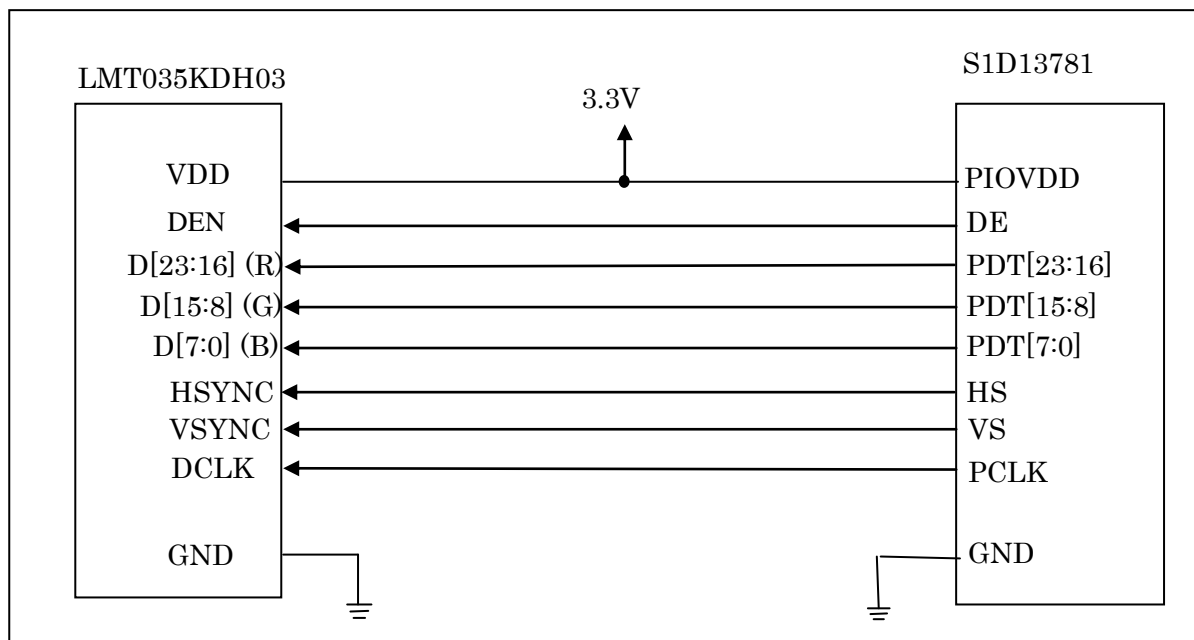


Figure 3-1 Connecting the LMT035KDH03 to the S1D13781

The following table provides a detailed pin listing for the required connections between the LMT035KDH03 and the S1D13781.

Table 3-2 Connecting the LMT035KDH03 to the S1D13781

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13781 QFP Pin#	S1D13781 Pin Name
1	LED_CATHODE	Backlight LED CATHODE Supply	—	—
2	LED_CATHODE	Backlight LED CATHODE Supply	—	—
3	LED_ANODE	Backlight LED ANODE Supply	—	—
4	LED_ANODE	Backlight LED ANODE Supply	—	—
5	NC	No Connection	—	—
6	NC	No Connection	—	—
7	NC	No Connection	—	—
8	/RES	Hardware Reset	—	—
9	/SPEN	SPI enable signal, active LOW, normal HIGH	—	—
10	SPCK	SPI clock signal, rising edge trigger	—	—
11	SPDA	SPI Data signal	—	—
12	D0	Blue data0	CN1-1	PDT0
13	D1	Blue data1	CN1-3	PDT1

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13781 QFP Pin#	S1D13781 Pin Name
14	D2	Blue data2	CN1-5	PDT2
15	D3	Blue data3	CN1-7	PDT3
16	D4	Blue data4	CN1-9	PDT4
17	D5	Blue data5	CN1-11	PDT5
18	D6	Blue data6	CN1-13	PDT6
19	D7	Blue data7	CN1-15	PDT7
20	D8	Green data0	CN1-17	PDT8
21	D9	Green data1	CN1-19	PDT9
22	D10	Green data2	CN1-21	PDT10
23	D11	Green data3	CN1-23	PDT11
24	D12	Green data4	CN1-25	PDT12
25	D13	Green data5	CN1-27	PDT13
26	D14	Green data6	CN1-29	PDT14
27	D15	Green data7	CN1-31	PDT15
28	D16	Red data0	CN1-4	PDT16
29	D17	Red data1	CN1-6	PDT17
30	D18	Red data2	CN2-3	PDT18
31	D19	Red data3	CN2-5	PDT19
32	D20	Red data4	CN2-7	PDT20
33	D21	Red data5	CN2-9	PDT21
34	D22	Red data6	CN2-11	PDT22
35	D23	Red data7	CN2-13	PDT23
36	HSYNC	Horizontal Sync Signal	CN1-37	HS
37	VSYNC	Vertical Sync Signal	CN1-39	VS
38	DCLK	Data Clock input	CN1-33	PCLK
39	NC	No Connection	—	—
40	NC	No Connection	—	—
41	VDD	Positive Power Supply	CN1-32	PIOVDD
42	VDD	Positive Power Supply	CN1-32	PIOVDD
43	NC	No Connection	—	—
44	NC	No Connection	—	—
45	NC	No Connection	—	—
46	NC	No Connection	—	—
47	NC	No Connection	—	—
48	NC	No Connection	—	—
49	NC	No Connection	—	—
50	NC	No Connection	—	—
51	NC	No Connection	—	—
52	DEN	Data Enable input	CN1-35	DE
53	GND	Power Ground Supply	CN1-2	GND

LCD Panel Connector Pin#	LCD Panel Pin Name	LCD Panel Pin Description	S1D13781 QFP Pin#	S1D13781 Pin Name
54	GND	Power Ground Supply	CN1-2	GND

Note

Allocation of GND and PIOVDD pin for each package is as follows.

GND: QFP 12, 23, 38, 48, 57, 67, 80, 90

PIOVDD: QFP 60, 73, 89

3.3 Example Register Settings

In addition to the pin connections, the S1D13781 internal registers must be configured appropriately for the LMT035KDH03 LCD panel. The following tables provide example settings for each display controller.

Also included in the table is an example clock configuration designed to achieve a typical LCD refresh.

Table 3-3 Example Register Settings for the S1D13781

Register Index and Name	Register Setting	Parameter Value
REG[10h] PLL Setting Register 0	0001h	PLL enable
REG[12h] PLL Setting Register 1	000Bh	MM=12
REG[14h] PLL Setting Register 2	0020h	LL=33
REG[16h] Internal Clock Configuration Register	0008h	fPLL_REF_CLK = fCLKI/9
REG[20h] Panel Setting Register	006Fh	DE: Hi-active PCLK Polarity: Falling edge PanelType: Color TFT 24-bit
REG[24h] Horizontal Display Width Register	0028h	320
REG[26h] Horizontal Non-Display Period Register	0066h	102
REG[28h] Vertical Display Height Register	00F0h	240
REG[2Ah] Vertical Non-Display Period Register	0021h	33
REG[04h] Power Save Configuration Register	0002h	MCK,PCLK enable
REG[22h] Display Setting Register	0001h	Panel interface enable
CLKI in MHz	—	24
PCLK in MHz	—	7.3
LCD refresh in Hz	—	63.36

Note

Parameter values are determined using a formula based on the register setting. For details on configuring the S1D13781 register values, see the *S1D13781 Hardware Functional Specification*, document number X92A-G-001-xx.

4 Change Record

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