



深圳市拓普微科技开发有限公司

SHENZHEN TOPWAY TECHNOLOGY CO., LTD.

LMT028DHHFWL-NEA

LCD Module User Manual

Prepared by: Gonghuimei Date: 2021-09-29	Checked by: Date:	Approved by: Date:
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Rev.	Descriptions	Release Date
0.1	Preliminary new release	2019-05-09
0.2	Add LED Backlight Circuit Characteristics	2021-09-29

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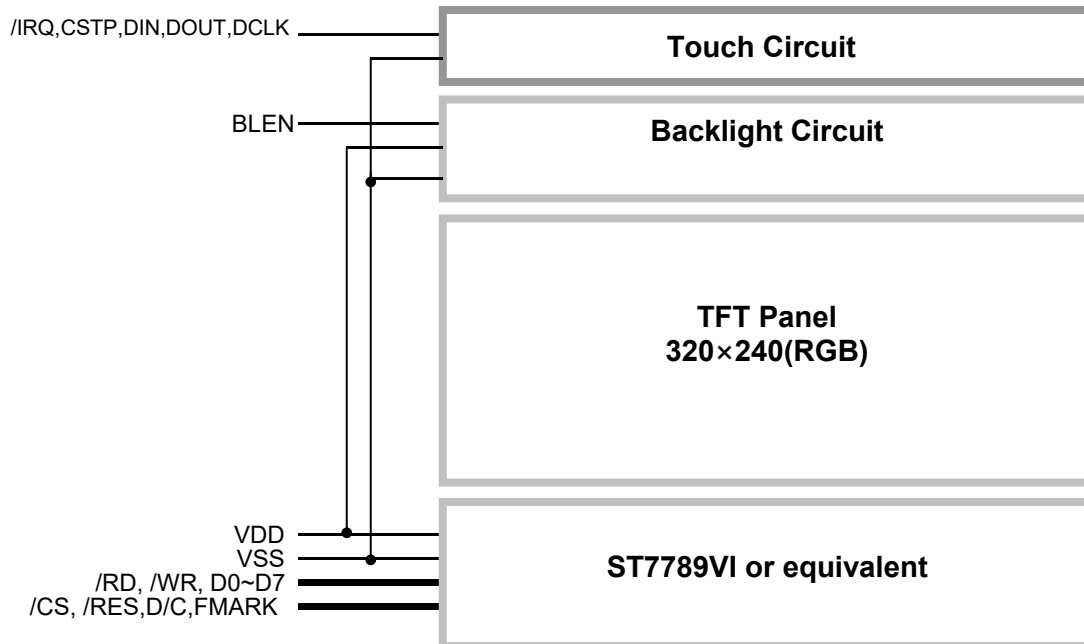
1. Basic Specifications

Screen Size(Diagonal) :	2.8"
Color Depth:	65k colors
Number of dots :	320 x 240(RGB)
Active Area :	57.6x43.2 mm
Dot Pitch :	0.18x0.18 mm
Display Technology :	a-Si TFT active matrix
Display Mode :	Transmissive / Positive
Pixel Configuration :	RGB Stripe
Viewing Direction :	3H (*1) (gray scale inverse) 9H (*2)
Polarizer Surface Treatment:	Glare
Backlight Type:	LEDs
Outline Dimension :	79.3 x 49.1 x 8.0(Max) mm (see dwg for details)
Operating Temperature :	-20 ~ +70°C
Storage Temperature :	-30 ~ +80°C

Note:

- *1. For saturated color display content (eg. pure-red, pure-green, pure-blue, or pure-colors-combinations).
- *2. For "color scales" display content.
- *3. Color tone may slightly change by Temperature and Driving Condition.

1.1 Block Diagram



1.2 Terminal Functions

Pin No. (K1)	Pin Name	I/O	Descriptions
1	VSS	P	Negative power supply,0V
2	VSS		
3	BLEN	I	Backlight control Program dimming levels by driving pin with digital pulses.
4	VDD	P	Positive power supply
5	VDD		
6	/RD	I	Read enable input, active low
7	/WR	I	Write enable input, active low
8	D/C	I	Register Select D/C=H, Transferring the Display Data D/C = L, Transferring the Control Data
9	/CS	I	Chip Select /CS=L, enable access to the LCD module /CS=H, disable access to the LCD module
10	D0	I/O	Data Input
:	:	:	:
17	D7	I/O	Data Input
18	/RES	I	Reset signal /RES = L, Initialization is executed /RES = H, Normal running.
19	FMARK	O	Displaying Timing Frame Signal
20	NC	-	No Connection
21	VSS	P	Negative power supply,0V
22	/IRQ	O	Pen Interrupt. Open anode output (requires 10kΩto 100kΩ pull-up resistor externally).
23	CSTP	O	Chip Select Input. Controls conversion timing and enables the serial input/output register.
24	DIN	I	Serial Data Input. If CS is LOW, data is latched on rising edge of DCLK.
25	DOUT	O	Serial Data Output. Data is shifted on the falling edge of DCLK. This output is high impedance when CS is HIGH.
26	DCLK	O	External Clock Input. This clock runs the SAR conversion process and synchronizes serial data I/O.

Pin No. (K2)	Pin Name	I/O	Descriptions
1	VSS	P	Negative power supply,0V
2	/IRQ	O	Pen Interrupt. Open anode output (requires 10kΩto 100kΩ pull-up resistor externally).
3	CSTP	O	Chip Select Input. Controls conversion timing and enables the serial input/output register.
4	DIN	I	Serial Data Input. If CS is LOW, data is latched on rising edge of DCLK.
5	DOUT	O	Serial Data Output. Data is shifted on the falling edge of DCLK. This output is high impedance when CS is HIGH.
6	DCLK	O	External Clock Input. This clock runs the SAR conversion process and synchronizes serial data I/O.
7	VSS	P	Negative power supply,0V
8	VSS		
9	BLEN	I	Backlight control Program dimming levels by driving pin with digital pulses.
10	VDD	P	Positive power supply
11	VDD		
12	/RD	I	Read enable input, active low
13	/WR	I	Write enable input, active low
14	D/C	I	Register Select D/C=H, Transferring the Display Data D/C = L, Transferring the Control Data
15	/CS	I	Chip Select /CS=L, enable access to the LCD module /CS=H, disable access to the LCD module
16	D0	I/O	Data Input
:	:	:	:
23	D7	I/O	Data Input
24	/RES	I	Reset signal /RES = L, Initialization is executed /RES = H, Normal running.
25	FMARK	O	Displaying Timing Frame Signal
26	NC	-	No Connection

2. Absolute Maximum Ratings

VDD =5V, VSS=0V, T_{OP}=25°C

Items	Symbol	Min.	Max.	Unit	Condition
Supply Voltage	VDD	-0.3	+5.5	V	VSS= 0V
Input Voltage	V _{IN}	-0.3	+4.6	V	VSS = 0V
Operating Temperature	T _{OP}	-20	+70	°C	No Condensation
Storage Temperature	T _{ST}	-30	+80	°C	No Condensation

Cautions:

Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

3. Electrical Characteristics

3.1 DC Characteristics

VDD=5V, VSS=0V, T_{OP}=25°C

Items	Symbol	MIN.	TYP.	MAX.	Unit	Condition / Application Pin
Operating Voltage	VDD	4.8	5.0	5.2	V	VDD
	IOVDD	2.7	3.0	3.6	V	IOVDD
Input High Voltage	V _{IH}	0.7* IOVDD	-	IOVDD	V	/RES,D0~D7,/CS,/RD, /WR,BLEN,D/C,
Input Low Voltage	V _{IL}	0	-	0.3* IOVDD	V	/IRQ,CSTP,DIN,DOUT, DCLK
Output High Voltage	V _{OH}	0.7* IOVDD	-	IOVDD	V	D0~D7, /IRQ,CSTP,DIN,DOUT, DCLK
Output Low Voltage	V _{OL}	0	-	0.3* IOVDD	V	D0~D7
		0	-	0.4* IOVDD	V	/IRQ,CSTP,DIN,DOUT, DCLK
Operating Current	I _{DD}	-	74.5	86	mA	Backlight are ON
	I _{DD}	-	6.25	16	mA	Backlight are OFF

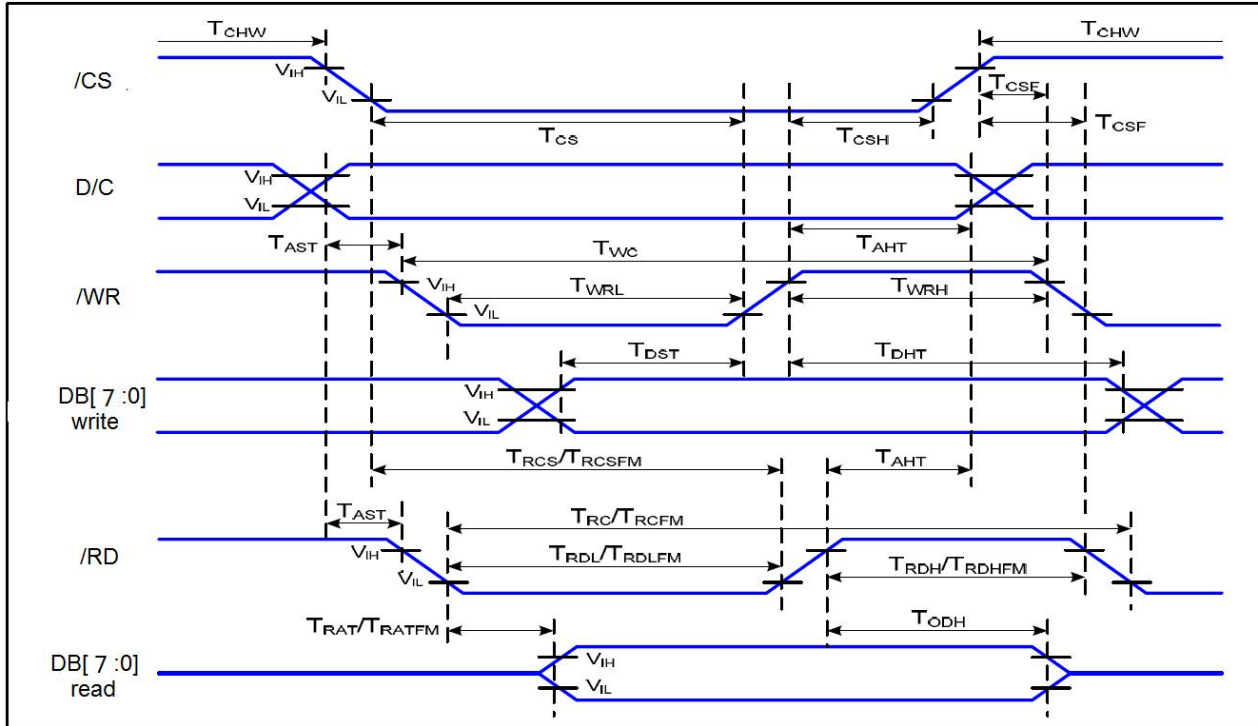
3.2 LED Backlight Circuit Characteristics

T_{OP}=25°C

Items	Symbol	MIN.	TYP.	MAX.	Unit	Remark
Forward Current	I _f	-	20	-	mA	For each LED
Backlight Power Consumption	W _{BL}	-	256	-	mW	4 LEDs
Operating Life Time	-	-	30,000	-	Hrs	For each LED

3.3 AC Characteristics

8080 Mode System Bus Timing



VDD =5V, VSS=0V, T_{OP}=25°C

Signal	Symbol	Parameter	Spec.		Unit	Description
			Min.	Max.		
D/C	T _{AST}	Address setup time	5	-	ns	-
	T _{AHT}	Address hole time(Write/Read)	13	-		
/CS	T _{CHW}	Chip select "H" pulse width	5	-	ns	-
	T _{CS}	Chip select setup time(Write)	20	-		
	T _{RCS}	Chip select setup time(Read ID)	60	-		
	T _{RCSFM}	Chip select setup time(Read FM)	460	-		
	T _{CSF}	Chip select wait time(Write/Read)	13	-		
	T _{CSH}	Chip select hold time	13	-		
/WR	T _{WC}	Write cycle	86	-	ns	-
	T _{WRH}	Control pulse "H" duration	20	-		
	T _{WRL}	Control pulse "L" duration	20	-		
DB[7:0]	T _{DST}	Data setup time	13	-	ns	For maximum CL=30pF For minimum CL=8pF
	T _{DHT}	Data hold time	13	-		
	T _{RAT}	Read access time(ID)	-	52		
	T _{RATFM}	Read access time(FM)	-	442		
	T _{ODH}	Ouput disable time	14	104		
/RD(ID)	T _{RC}	Read cycle(ID)	208	-	ns	When read ID data
	T _{RDH}	Control pulse "H" duration(ID)	120	-		
	T _{RDL}	Control pulse "H" duration(ID)	60	-		
/RD(FM)	T _{RCFM}	Read cycle(FM)	585	-	ns	When read from frame memory
	T _{RDHFM}	Control pulse "H" duration(FM)	120	-		
	T _{RDLFM}	Control pulse "H" duration(FM)	460	-		

Note:

- *1. Input signal rise/fall time should be less than 15ns .
- *2. All timing is using 20% and 80% of VDD as the reference.
- *3. Please refer to ST7789VI datasheet for details

3.4 Touch Panel controller Timing Characteristics

VDD=5V, VSS=0V, T_{OP}=25°C

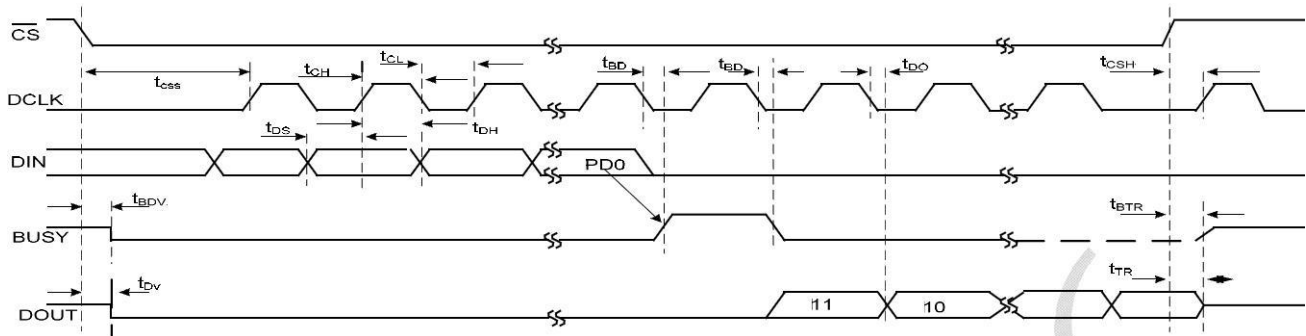
Item	Symbol	MIN.	TYP.	MAX.	Unit
Acquisition time(*1)	t _{ACQ}	1.5	-	-	us
DIN Valid Prior to DCLK Rising	t _{DS}	100	-	-	ns
DIN Hold After DCLK HIGH	t _{DH}	50	-	-	ns
DCLK Falling to DOUT Valid	t _{DO}	-	-	200	ns
CSTP Falling to DOUT Enabled	t _{DV}	-	-	200	ns
CSTP Rising to DOUT Disabled	t _{TR}	-	-	200	ns
CSTP Falling to First DCLK Rising	t _{CSS}	100	-	-	ns
CSTP Rising to DCLK Ignored	t _{CSH}	10	-	-	ns
DCLK high pulse width	t _{CH}	200	-	-	ns
DCLK low pulse width	t _{CL}	200	-	-	ns
DCLK Falling to BUSY Rising	t _{BD}	-	-	200	ns
CSTP Falling to BUSY Enabled	t _{BDV}	-	-	200	ns
CSTP Rising to BUSY Disabled	t _{BTR}	-	-	200	ns

NOTE:

*1 See Serial Data Sequence Diagram.

*2 The BUSY signal is not connected to Terminal (K3,K4),after one control byte send via DIN, some delay is needed to read the conversation result through DOUT.

*3 Please see the XPT2046 datasheet for details.



Timing diagram

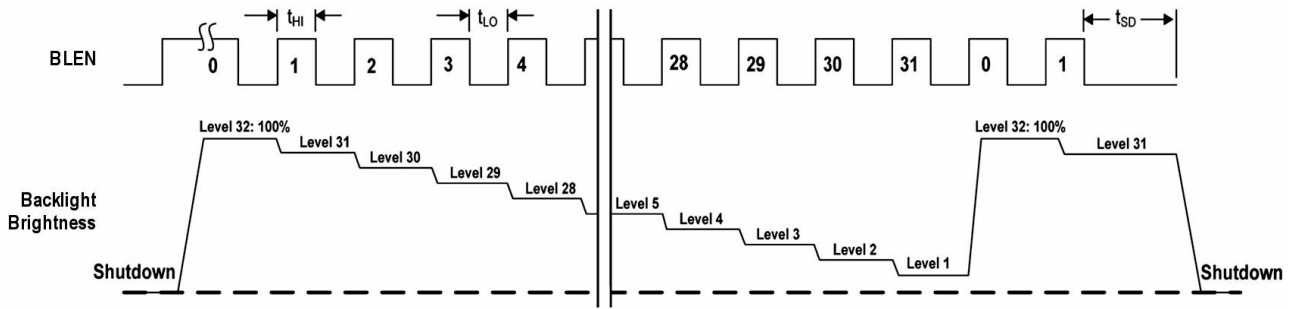
3.5 Backlight control Timing

VDD=5V, VSS=0V, T_{OP} =25°C

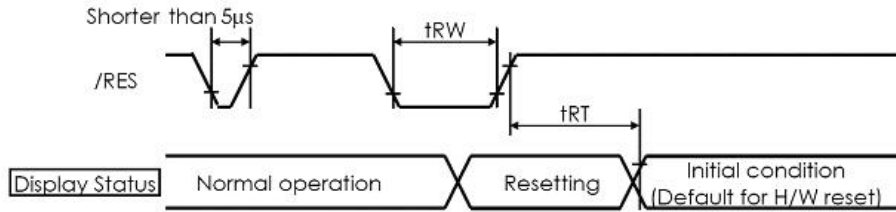
Signal	Symbol	Parameter	Spec.			Unit	Description
			Min.	Typ	Max.		
BLEN	t _{HI}	Time Delay between Steps	2	-	-	us	H: 3.3V
	t _{LO}	CTRL LOW Time for Dimming	1	-	250	us	L: 0V
	t _{SD}	CTRL LOW ,shutdown Pulse Whidth	2	-	-	ms	

Note: For basic ON/OFF function, please beware of minimum pulse width.

Register BLEN timing



3.6 Reset Timing



VDD =5V, VSS=0V, T_{OP}=25°C

Item	Symbol	MIN.	TYP.	MAX.	Unit
Reset LOW pulse width	t _{RW}	10	-	-	us
Reset time	T _{RT}	-	-	170	ms

4. Functions

4.1 Display Commands

Instruction	D/C	/WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
NOP	0	↑	-	0	0	0	0	0	0	0	0	(00h)	No operation
SWRESET	0	↑	-	0	0	0	0	0	0	0	1	(01h)	Software reset
RDDID	0	↑	-	0	0	0	0	0	1	0	0	(04h)	Read display ID
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		ID1 read
	1	1	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		ID2 read
	1	1	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		ID3 read
RDDST	0	↑	-	0	0	0	0	1	0	0	1	(09h)	Read display status
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24		-
	1	1	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON		-
	1	1	-	ST15	ST14	INVON	ST12	ST11	DISON	TEON	GCS2		-
	1	1	-	GCS1	GCS0	TEM	ST4	ST3	ST2	ST1	ST0		-
RDDPM	0	↑	-	0	0	0	0	1	0	1	0	(0Ah)	Read display power
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	-	BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	0	0		
RDD MADCTL	0	↑	-	0	0	0	0	1	0	1	1	(0Bh)	Read display
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	-	MY	MX	MV	ML	RGB	MH	0	0		-
RDD COLMOD	0	↑	-	0	0	0	0	1	1	0	0	(0Ch)	Read display pixel
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	-	0	D6	D5	D4	0	D2	D1	D0		-
RDDIM	0	↑	-	0	0	0	0	1	1	0	1	(0Dh)	Read display image
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	-	VSSON	0	INVON	0	0	GC2	GC1	GC0		-
RDDSM	0	↑	-	0	0	0	0	1	1	1	0	(0Eh)	Read display signal
	1	1	-	-	-	-	-	-	-	-	-		Dummy read

Instruction	D/C	/WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	1	-	TEON	TEM	0	0	0	0	0	0		-
RDDSDR	0	↑	-	0	0	0	0	1	1	1	1	(0Fh)	Read display self-diagnostic result
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	-	D7	D6	0	0	0	0	0	0		-
SLPIN	0	↑	-	0	0	0	1	0	0	0	0	(10h)	Sleep in
SLPOUT	0	↑	-	0	0	0	1	0	0	0	1	(11h)	Sleep out
PTLON	0	↑	-	0	0	0	1	0	0	1	0	(12h)	Partial mode on
NORON	0	↑	-	0	0	0	1	0	0	1	1	(13h)	Partial off (Normal)
INVOFF	0	↑	-	0	0	1	0	0	0	0	0	(20h)	Display inversion off
INVON	0	↑	-	0	0	1	0	0	0	0	1	(21h)	Display inversion on
GAMSET	0	↑	-	0	0	1	0	0	0	0	1	(26h)	Display inversion on
	1	↑	-	0	0	0	0	GC3	GC2	GC1	GC0		
DISPOFF	0	↑	-	0	0	1	0	1	0	0	0	(28h)	Display off
DISPON	0	↑	-	0	0	1	0	1	0	0	1	(29h)	Display on
CASET	0	↑	-	0	0	1	0	1	0	1	0	(2Ah)	Column address set
	1	↑	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8		X address start:
	1	↑		XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0		$0 \leq XS \leq X$
	1	↑		XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8		X address start:
	1	↑		XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0		$S \leq XE \leq X$
RASET	0	↑	-	0	0	1	0	1	0	1	1	(2Bh)	Row address set
	1	↑	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8		Y address start:
	1	↑		YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0		$0 \leq YS \leq Y$
	1	↑		YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8		Y address start:
	1	↑		YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0		$S \leq YE \leq Y$
RAMWR	0	↑	-	0	0	1	0	1	1	0	0	(2Ch)	Memory write
	1	↑	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Write data
	1	↑	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	↑	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
RAMRD	0	↑	-	0	0	1	0	1	1	1	0	(2Eh)	Memory read

Instruction	D/C	/WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Read data
	1	1	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	1	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
PTLAR	0	↑	-	0	0	1	1	0	0	0	0	(30h)	Partial start/end address set
	1	↑	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8		Partial start address: (0, 1, 2, ..P)
	1	↑	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0		
	1	↑	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8		Partial end address (0, 1, 2, 3, , P)
1	↑	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0			
VSCRDEF	0	↑	-	0	0	1	1	0	0	1	1	(33h)	Vertical scrolling definition
	1	↑	-	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8		
	1	↑	-	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0		
	1	↑	-	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8		
	1	↑	-	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0		
	1	↑	-	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8		
	1	↑	-	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0		
TEOFF	0	↑	-	0	0	1	1	0	1	0	0	(34h)	Tearing effect line off
TEON	0	↑	-	0	0	1	1	0	1	0	1	(35h)	Tearing effect line on
	1	↑	-	-	-	-	-	-	-	-	TEM		
MADCTL	0	↑	-	0	0	1	1	0	1	1	0	(36h)	Memory data access control
	1	↑	-	MY	MX	MV	ML	RGB	0	0	0		-
VSCRSADD	0	↑	-	0	0	1	1	0	1	1	1	(37h)	Vertical scrolling start address
	1	↑	-	VSP15	VSP14	VSP13	VSP12	VSP11	VSP10	VSP9	VSP8		
	1	↑	-	VSP7	VSP6	VSP5	VSP4	VSP3	VSP2	VSP1	VSP0		
IDMOFF	0	↑	-	0	0	1	1	1	0	0	0	(38h)	Idle mode off
IDMON	0	↑	-	0	0	1	1	1	0	0	1	(39h)	Idle mode on
COLMOD	0	↑	-	0	0	1	1	1	0	1	0	(3Ah)	Interface pixel format

Instruction	D/C	/WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	↑	-	0	D6	D5	D4	0	D2	D1	D0		Interface format
RAMWRC	0	↑	-	0	0	1	1	1	1	0	0	(3Ch)	Memory write continue
	1	↑	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Write data
	1	↑	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	↑	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
RAMRDC	0	↑	-	0	0	1	1	1	1	1	0	(3Eh)	Memory read continue
	1	1	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		
	1	1	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	1	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
TESCAN	0	↑	-	0	1	0	0	0	1	0	0	(44h)	Set tear scanline
	1	↑	-	N15	N14	N13	N12	N11	N10	N9	N8		
	1	↑	-	N7	N6	N5	N4	N3	N2	N1	N0		
RDTESCAN	0	↑	-	0	1	0	0	0	1	0	1	(45h)	Get scanline
	1	1	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	-	-	-	-	-	-	-	N9	N8		
	1	1	-	N7	N6	N5	N4	N3	N2	N1	N0		
WRDISBV	0	↑	-	0	1	0	1	0	0	0	1	(51h)	Write display brightness
	1	↑	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0		
RDDISBV	0	↑	-	0	1	0	1	0	0	1	0	(52h)	Read display brightness value
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0		
WRCTRLD	0	↑	-	0	1	0	1	0	0	1	1	(53h)	Write CTRL display
	1	↑	-	0	0	BCTRL	0	DD	BL	0	0		
RDCTRLD	0	↑	-	0	1	0	1	0	1	0	0	(54h)	Read CTRL value display
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	-	0	0	BCTRL	0	DD	BL	0	0		

Instruction	D/C	/WR	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
WRCACE	0	↑	-	0	1	0	1	0	1	0	1	(55h)	Write content adaptive brightness control and Color enhancemnet
	1	↑	-	CECTRL	0	CE1	CE0	0	0	C1	C0		
RDCABC	0	↑	-	0	1	0	1	0	1	1	0	(56h)	Read content adaptive brightness control
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	-	0	CECTRL	0	0	0	0	C1	C0		
WRCABCMB	0	↑	-	0	1	0	1	1	1	1	0	(5Eh)	Write CABC minimum brightness
	1	↑	-	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0		
RDCABCMB	0	↑	-	0	1	0	1	1	1	1	1	(5Fh)	Read CABC minimum brightness
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	-	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0		
RDID1	0	↑	-	1	1	0	1	1	0	1	0	(Dah)	Read ID1
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		Read parameter
RDID2	0	↑	-	1	1	0	1	1	0	1	1	(DBh)	Read ID2
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		Read parameter
RDID3	0	↑	-	1	1	0	1	1	1	0	0	(DCh)	Read ID3
	1	1	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		Read parameter

Notes:

1. There will be no abnormal visible effects on the display when S/W or H/W Reset are applied.
2. Please refer to ST7789V1 datasheet for details

4.2 Power off the LCD Module

It recommends that enter Sleep Mode before power off the LCD module.

4.3 Refreshing The LCD Module

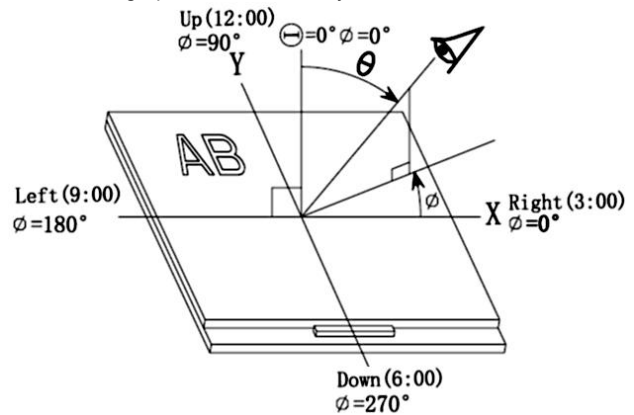
It recommends that the operating modes and display contents be refreshed periodically to prevent the effect of unexpected noise.

5. Optical Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	UNIT	Note.
Viewing angle	$\Phi=90^\circ$	$(CR \geq 10)$	50	60	-	degree	Note 1,6
	$\Phi=270^\circ$		50	60	-		
	$\Phi=180^\circ$		40	50	-		
	$\Phi=0^\circ$		50	60	-		
Contrast ratio	CR	$\Phi=0^\circ$ $\theta=0^\circ$	300	500	-	-	Note 3
Response Time	T_{on}	$\Phi=0^\circ$ $\theta=0^\circ$	-	30	50	msec	Note 4
	T_{off}					msec	
Chromaticity	Red	Backlight is on $\Phi=0^\circ$ $\theta=0^\circ$	X	0.55	0.60	0.65	Note 1,5
			Y	0.30	0.35	0.40	
	Green		X	0.27	0.32	0.37	
			Y	0.56	0.61	0.66	
	Blue		X	0.09	0.14	0.19	
			Y	0.05	0.09	0.15	
	White		X	0.26	0.29	0.32	
			Y	0.28	0.31	0.34	
NTSC Ratio	S		45	65	-	%	
Luminance	L	$\Phi=0^\circ$	160	200	-	cd/m ²	Note 1,6
Luminance uniformity	U	$\theta=0^\circ$	80	-	-	%	Note 1,6

Note 1:
 The data are measured after LEDs are turned on for 5 minutes. LCM displays full white. The brightness is the average value of 9 measured spots. Measurement equipment PR-705
Measuring condition:
 - Measuring surroundings: Dark room
 - Measuring temperature: Ta=25°C.
 - Adjust operating voltage to get optimum contrast at the center of the display.

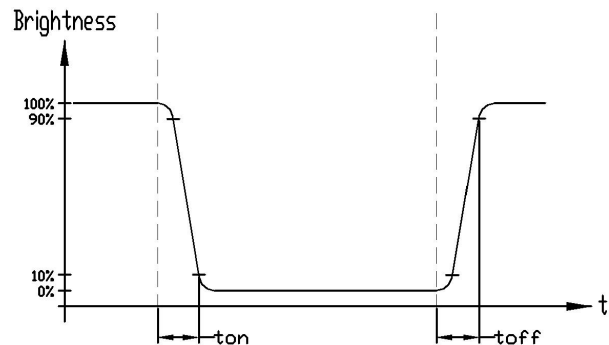
Note 2:
 The definition of viewing angle:
 Refer to the graph below marked by θ and ϕ



Note 3:
 The definition of contrast ratio (Test LCM using PR-705):

$$\text{Contrast Ratio (CR)} = \frac{\text{Luminance When LCD is at "White" state}}{\text{Luminance When LCD is at "Black" state}}$$
 (Contrast Ratio is measured in optimum common electrode voltage)

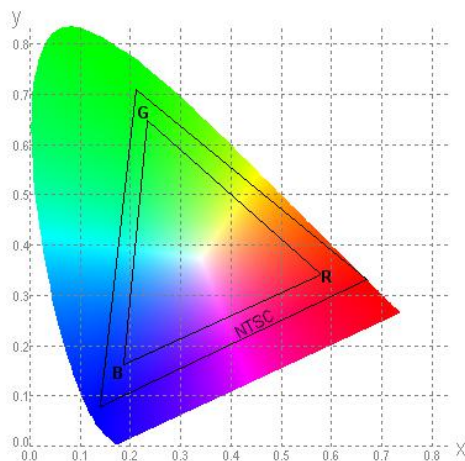
Note 4:
 Definition of Response time. (Test LCD using DMS501):
 The output signals of photo detector are measured when the input signals are changed from "black" to "white" (falling time) and from "white" to "black" (rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 5:
 Definition of Color of CIE1931 Coordinate and NTSC Ratio.

Color gamut:

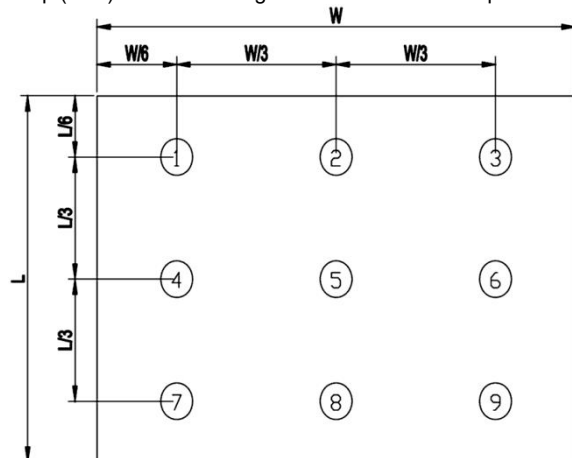
$$S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$$



Note 6:
 The luminance uniformity is calculated by using following formula.

$$\Delta Bp = Bp (\text{Min.}) / Bp (\text{Max.}) \times 100 (\%)$$

 Bp (Max.) = Maximum brightness in 9 measured spots
 Bp (Min.) = Minimum brightness in 9 measured spots.



Note 7:
 Measured the luminance of white state at center point

6. LCD Module Design and Handling Precautions

- Please ensure V0, VCOM is adjustable, to enable LCD module get the best contrast ratio under different temperatures, view angles and positions.
- Normally display quality should be judged under the best contrast ratio within viewable area. Unexpected display pattern may come out under abnormal contrast ratio.
- Never operate the LCD module exceed the absolute maximum ratings.
- Never apply signal to the LCD module without power supply.
- Keep signal line as short as possible to reduce external noise interference.
- IC chip (e.g. TAB or COG) is sensitive to light. Strong light might cause malfunction. Light sealing structure casing is recommended.
- Make sure there is enough space (with cushion) between case and LCD panel, to prevent external force passed on to the panel; otherwise that may cause damage to the LCD and degrade its display result.
- Avoid showing a display pattern on screen for a long time (continuous ON segment).
- LCD module reliability may be reduced by temperature shock.
- When storing and operating LCD module, avoids exposure to direct sunlight, high humidity, high or low temperature. They may damage or degrade the LCD module.
- Never leave LCD module in extreme condition (max./min storage/operate temperature) for more than 48hr.
- Recommend LCD module storage conditions is 0 C~40 C <80%RH.
- LCD module should be stored in the room without acid, alkali and harmful gas.
- Avoid dropping & violent shocking during transportation, and no excessive pressure press, moisture and sunlight.
- LCD module can be easily damaged by static electricity. Please maintain an optimum anti-static working environment to protect the LCD module. (eg. ground the soldering irons properly)
- Be sure to ground the body when handling LCD module.
- Only hold LCD module by its sides. Never hold LCD module by applying force on the heat seal or TAB.
- When soldering, control the temperature and duration avoid damaging the backlight guide or diffuser which might degrade the display result such as uneven display.
- Never let LCD module contact with corrosive liquids, which might cause damage to the backlight guide or the electric circuit of LCD module.
- Only clean LCD with a soft dry cloth, Isopropyl Alcohol or Ethyl Alcohol. Other solvents (e.g. water) may damage the LCD.
- Never add force to components of LCD module. It may cause invisible damage or degrade the module's reliability.
- When mounting LCD module, please make sure it is free from twisting, warping and bending.
- Do not add excessive force on surface of LCD, which may cause the display color change abnormally.
- LCD panel is made with glass. Any mechanical shock (e.g.

6. 液晶显示模块设计和使用须知

- 请注意 V0, VCOM 的设定, 以确保液晶显示模块在不同的使用温度下以及在不同的视角和位置观察模块显示, 均能达到最佳对比度, 请务必将应用电路上设置为对比度可调。
- 请注意液晶显示模块的显示品质判定是指在正常对比度下以及视窗 (V. A) 范围内进行的, 非正常对比度下液晶可能会出现非预期的显示不良, 应注意区分。
- 请勿在最大额定值以外使用液晶显示模块。
- 请勿在没有接通电源的条件下, 给液晶显示模块输送信号。
- 请尽可能缩短信号线的连接, 以避免对液晶显示模块的信号干扰。
- 集成电路 IC 芯片 (如 TAB 或 COG) 对紫外线极为敏感, 强光环境下可能会引起液晶显示模块功能失效, 故应采用不透光的外壳。
- 请在液晶显示模块与外壳之间保留足够的空间 (可使用衬垫), 以缓冲外力对液晶显示模块的损坏或因受力不均而产生的显示不均匀等异常现象。
- 避免液晶显示屏在某一画面下长时间点亮, 否则有出现残影的风险; 请通过软件每隔一段时间改变一次画面。
- 液晶显示模块的可靠性可能因温度冲击而降低。
- 请勿在阳光直射、高湿、高温或低温下储存和使用液晶显示模块, 这将造成液晶显示模块的损坏或失效。
- 请勿在极限环境 (最大/最小存储/工作温度) 下使用或放置液晶显示模块超过 48 小时以上。
- 液晶显示模块建议存储条件为: 0 C~40 C <80%RH。
- 请勿让液晶显示模块存储于带有酸性, 碱性, 有害气体环境之中。
- 在运输过程中, 请勿让液晶显示模块跌落与猛烈震动, 同时避免异常挤压, 高湿度, 与阳光照射。
- 液晶显示模块极易受静电损坏, 请务必保证液晶显示模块在防静电的工作环境中使用或保存。(如: 烙铁正确接地, 等)
- 拿取液晶显示模块时需注意操作人员的接地情况。
- 请手持液晶显示模块的边沿取放模块, 防止热压纸或 TAB 部位受力。
- 焊接液晶模块时, 请注意控制烙铁的温度、焊接时间, 以免烫坏导光板或偏光片, 导致显示不均匀等不良现象发生。
- 请勿使用洗板水等腐蚀性液体接触液晶模块, 以免腐蚀导光板或模块电路。
- 仅可使用柔软的干布, 异丙醇或乙醇清洁液晶屏表面, 其他任何溶剂 (如: 水) 都有可能损坏液晶模块。
- 请勿挤压液晶显示模块上的元器件, 以避免产生潜在的损坏或失效而影响产品可靠性。
- 装配液晶显示模块时, 请务必注意避免液晶显示模块的扭曲或变形。
- 请勿挤压液晶显示屏表面, 这将导致显示颜色的异常。
- 液晶屏由玻璃制作而成, 任何机械碰撞 (如从高处跌落) 均有可能损坏液晶显示模块。

- dropping from high place) will damage the LCD module.
- Protective film is attached on LCD screen. Be careful when peeling off this protective film, since static electricity may be generated.
- Polarizer on LCD gets scratched easily. If possible, do not remove LCD protective film until the last step of installation.
- When peeling off protective film from LCD, static charge may cause abnormal display pattern. The symptom is normal, and it will turn back to normal in a short while.
- LCD panel has sharp edges, please handle with care.
- Never attempt to disassemble or rework LCD module.
- If display panel is damaged and liquid crystal substance leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes promptly wash it off using soap and water.

- 液晶屏表面带有保护膜，揭除保护膜时需要注意可能产生的静电。
- 因液晶显示屏表面的偏光片极易划伤，安装完成之前请尽量不要揭下保护膜。
- 请缓慢揭除保护膜，在此过程中液晶显示屏上可能会产生静电，此为正常情况，可在短时间内消失。
- 请注意避免被液晶显示屏的边缘割伤。
- 请不要试图拆卸或改造液晶显示模块。
- 当液晶显示屏出现破裂，内部液晶液体可能流出；相关液体不可吞吃，绝对不可接触嘴巴，如接触到皮肤或衣服，请使用肥皂与清水彻底清洗。

7. CTP Mounting Instructions

7.1 Bezel Mounting (Figure 1)

- The bezel window should be bigger than the CTP active area. It should be $\geq 0.5\text{mm}$ each side.
- Gasket should be installed between the bezel and the CTP surface. The final gap should be about $0.5\sim 1.0\text{mm}$.
- It is recommended to provide an additional support bracket for backside support when necessary (e.g. slim type TFT module without mounding structure). They should only provide appropriate support and keep the module in place.
- The mounting structure should be strong enough to prevent external uneven force or twist act onto the module.

7.1 面框安装 (附图 1)

- 客户面框窗口应大于 CTP 动作区域，各边离动作区应 $\geq 0.5\text{mm}$ 。
- 面框与 CTP 面板间应垫有胶垫，其最终间隙约为 $0.5\sim 1.0\text{mm}$ 。
- 建议必要时在背面提供附加支架 (例如无安装结构的薄型 TFT 模块)，应仅利用适当支撑以保持模块位置。
- 安装结构应具有足够的强度，以防止外部不均匀力或扭曲力作用到模块上。

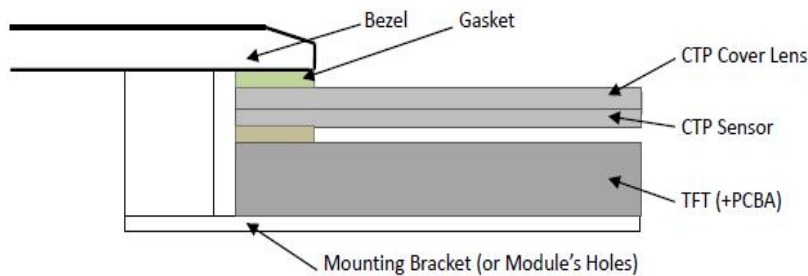


Figure 1

7.2 Surface Mounting (Figure 2)

- As the CTP assembling on the countersink area with double side adhesive. The countersink area should be flat and clean to ensure the double side adhesive installation result.
- The Bezel is recommend to keep a gap ($\geq 0.3\text{mm}$ each side) around the cover lens for tolerance.
- It is recommended to provide an additional support bracket with gasket for backside support when necessary (e.g. TFT module without mounding structure). They should only provide appropriate support and keep the module in place.
- The mounting structure should be strong enough to prevent external uneven force or twist act onto the module

7.2 嵌入安装 (附图 2)

- 客户面框应具有使用双面胶粘贴 CTP 的结构沉台面，其粘贴面要求平整且洁净无污染以保证粘贴牢靠。
- 考虑到制作误差，建议面框与 CTP 盖板之间四周留有 $\geq 0.3\text{mm}$ 间隙。
- 建议必要时在背面提供垫有胶垫附加支架 (例如无安装结构的 TFT 模块)，应仅利用适当支撑以保持模块位置。
- 安装结构应具有足够的强度，以防止外部不均匀力或扭曲力作用到模块上。

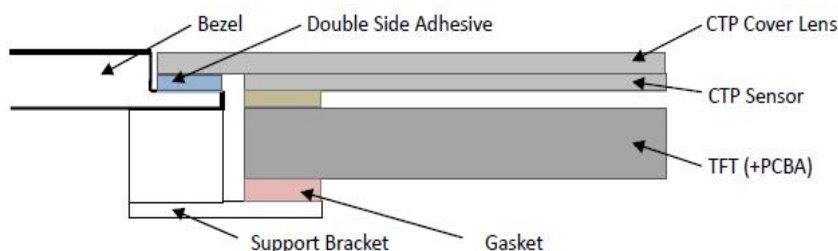


Figure 2

7.3 Additional Cover Lens Mounting (Figure 3)

- For the case of additional cover Lens mounting, it is necessary to recheck with the CTP specification about the material and thickness to ensure the functionality.
- It should keep a 0.2~0.3mm gap between the cover lens and the CTP surface..
- The cover lens window should be bigger than the active area of the CTP.It should be $\geq 0.5\text{mm}$ each side.
- It is recommended to provide an additional support bracket for backside support when necessary (e.g. slim type TFT module without mounding structure). They should only provide appropriate support and keep the module in place.
- The mounting structure should be strong enough to prevent external uneven force or twist act onto the module.

7.3 覆加盖板 (附图 3)

- 需要覆加玻璃盖板的安装, 为确保其功能, 有必要查看产品规格书中有关盖板材料和厚度的说明.
- 玻璃盖板与 CTP 表面之间应留有 0.2 ~ 0.3mm 间隙.
- 玻璃盖板视窗应大于 CTP 动作区域, 各边离动作区应 $\geq 0.5\text{mm}$.
- 建议必要时在背面提供附加支架 (例如无安装结构的薄型 TFT 模块), 应仅利用适当支撑以保持模块位置.
- 安装结构应具有足够的强度, 以防止外部不均匀力或扭曲力作用到模块上.

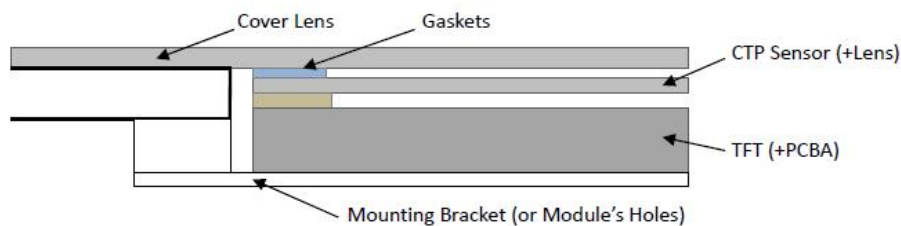


Figure 3

8. RTP Mounting Instructions

- It should bezel touching the RTP Active Area (A.A) to prevent abnormal touch.It should left gab $D=0.2\sim 0.3\text{mm}$ in between. (Figure 4)
- Outer bezel design should take care about the area outside the A.A. Those areas contain circuit wires which is having different thickness. Touching those areas could de-form the ITO film. As a result bezel the ITO film be damaged and shorten its lifetime. It is suggested to protect those areas with gasket (between the bezel and RTP).The suggested figures are $B\geq 0.50\text{mm}$; $C\geq 0.50\text{mm}$. (Figure 4)
- The bezel side wall should keep space $E= 0.2 \sim 0.3\text{mm}$ from the RTP. (Figure 4)

8. 电阻触摸屏安装指导

- 为避免面框直接压在动作区 (A. A.) 上造成误动作, 面框与电阻触摸屏 (RTP) 之间应留有一定的空隙 $D=0.2\sim 0.3\text{mm}$ 之间. (附图 4)
- 设计面框时, 要注意用面框保护触摸屏四周的非保证操作区域, 因为布线区域在此处形成一台阶, 在此区域附近操作时 ITO Film 变形较大, 容易导致 ITO 损坏而降低寿命. 为保护 RTP 和避免误操作, 在 RTP 与面框之间垫缓冲物 (Gasket), 我们建议设计面框应覆盖动作区的边缘, 面框边缘到 V. A. 区的距离 $B\geq 0.50\text{mm}$; 垫圈内边缘到 V. A. 区的距离 $C\geq 0.50\text{mm}$. (附图 4)
- 在设计面框与 RTP 组装时, 应考虑到面框内侧与 RTP 外侧的间距 $E\geq 0.2\text{mm}$. (附图 4)

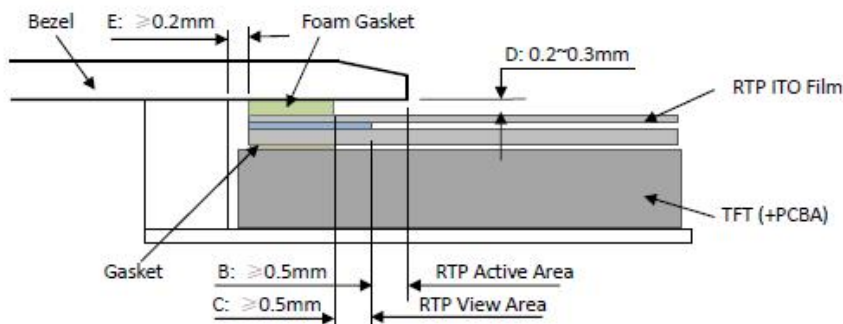


Figure 4

- In general design,

- 通常设计时:

RTP V.A. should be bigger than the TFT V.A.
and RTP A.A. should be bigger than the TFT A.A.
(Figure 5)

RTP 的可视区 V. A. 应不小于 TFT 的可视区 V. A.
及 RTP 的动作区 A. A. 应不小于 TFT 的动作区 A. A.
(附图 5)

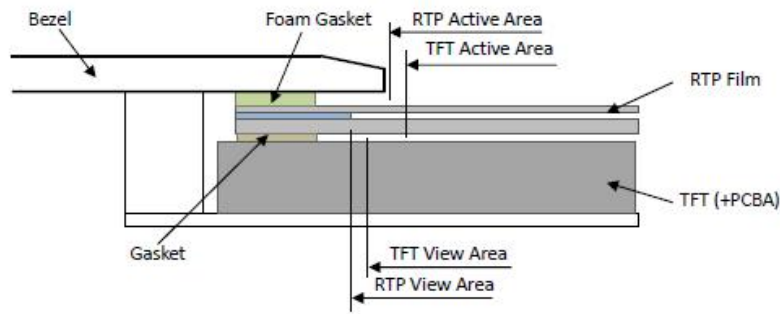
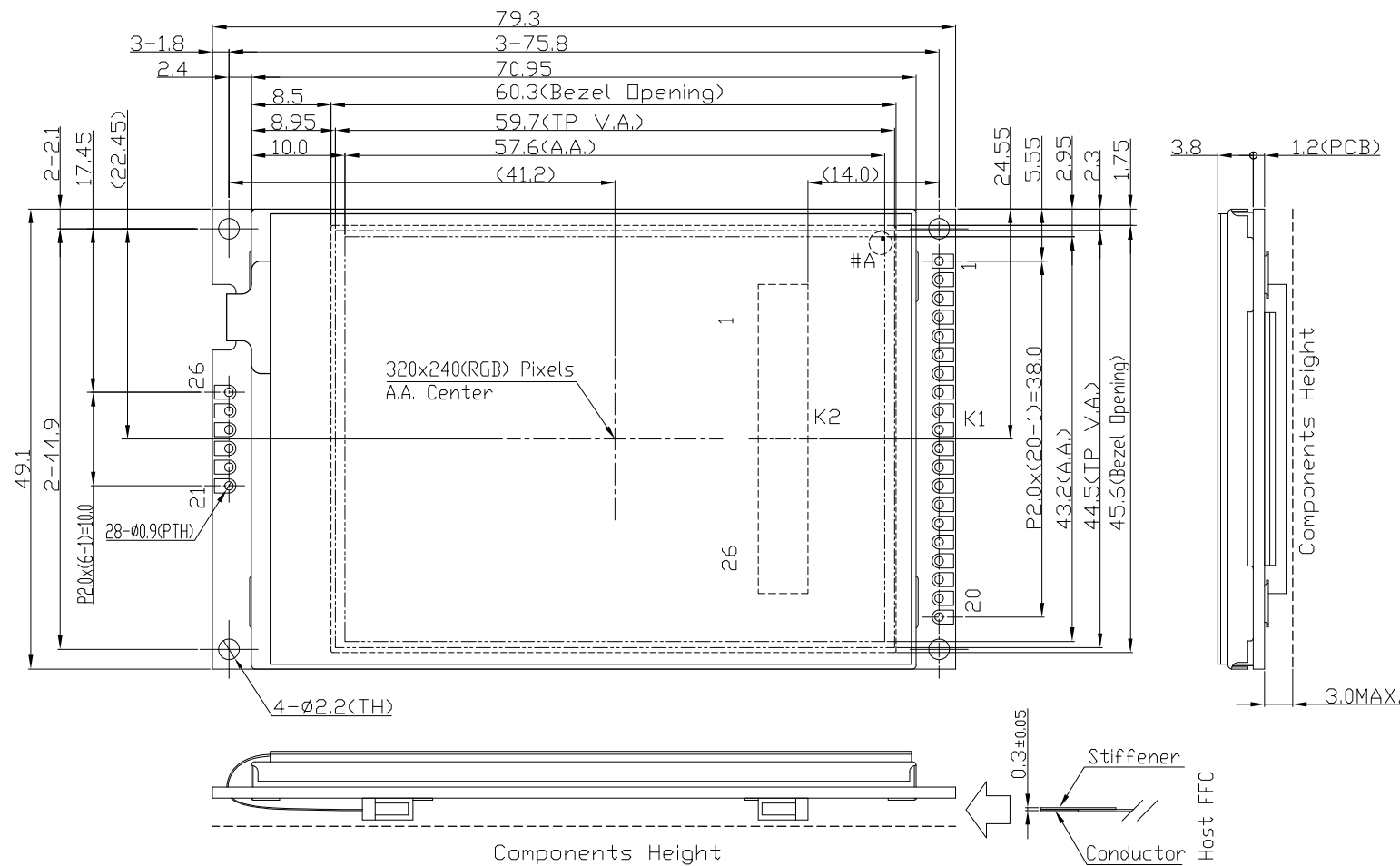


Figure 5

Warranty

This product has been manufactured to our company’s specifications as a part for use in your company’s general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we cannot take responsibility if the product is used in medical devices, nuclear power control equipment, aerospace equipment, fire and security systems, or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required. If the product is to be used in any of the above applications, we will need to enter into a separate product liability agreement.

- We cannot accept responsibility for any defect, which may arise from additional manufacturing of the product (including disassembly and reassembly), after product delivery.
- We cannot accept responsibility for any defect, which may arise after the application of strong external force to the product.
- We cannot accept responsibility for any defect, which may arise due to the application of static electricity after the product has passed our company’s acceptance inspection procedures.
- When the product is in CCFL models, CCFL service life and brightness will vary according to the performance of the inverter used, leaks, etc. We cannot accept responsibility for product performance, reliability, or defect, which may arise.
- We cannot accept responsibility for intellectual property of a third part, which may arise through the application of our product to our assembly with exception to those issues relating directly to the structure or method of manufacturing of our product.

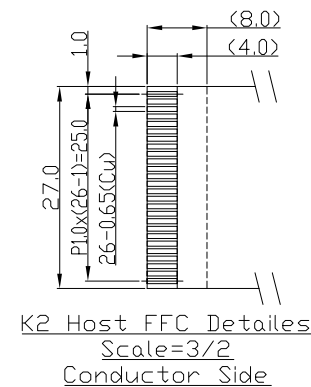
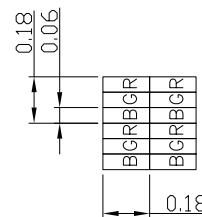


K1 Terminal		
No	Pin Name	
1	VSS	
2	VSS	
3	BLEN	
4	VDD	
5	VDD	
6	/RD	
7	/WR	
8	D/C	
9	/CS	
10	D0	
11	D1	
12	D2	
13	D3	
14	D4	
15	D5	
16	D6	
17	D7	
18	/RES	
19	FMARK	
20	NC	
21	VSS	
22	/IRQ	
23	CSTP	
24	DIN	
25	DDOUT	
26	DCLK	

K2 Terminal		
No	Pin Name	
1	VSS	
2	/IRQ	
3	CSTP	
4	DIN	
5	DDOUT	
6	DCLK	
7	VSS	
8	VSS	
9	BLEN	
10	VDD	
11	VDD	
12	/RD	
13	/WR	
14	D/C	
15	/CS	
16	D0	
17	D1	
18	D2	
19	D3	
20	D4	
21	D5	
22	D6	
23	D7	
24	/RES	
25	FMARK	
26	NC	

Note:

- *1. LCD Display Type : TFT, Transmissive
- *2. Operating Voltage : 5.0V, Logic Voltage : 3.3V
- *3. Backlight : White LEDs
- *4. Pixel Arrangement : RGB-STRIPE
- *5. Color Depth : 65k Colors
- *6. Signal Interface : MCU 8bit
- *7. Touch Panel Type : Resistive Touch Panel
- *8. Connector:
 - K1: P2.0,1x20+1x6 PCB Pad
 - K2: 26Pin P1.0 FFC Socket Or Equivalent
- *9. Operating Temperature : -20°C~70°C
- *10. Storage Temperature : -30°C~80°C
- *11. Foam Gasket must be assemble outside RTP VA by 0.5mm



C			
B			
A			
Rev	Note	Date	
Dwg title LMT028DHHFWL-NEA Outline Dwg			
Dwg No.	MK-006552-1-1	Date	2019-03-06
Scale	2/1	Tol.	±0.5
Unit	mm	Paper Size	A3
Approved	Checked	Drawn Luo Lin	

TOPWAY