深圳市拓普微科技开发有限公司
SHENZHEN TOPWAY TECHNOLOGY CO., LTD.

LMT035DNJFWD-NND

LCD Module User Manual

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Date: 2024-01-03	Date:	Date:

Rev.	Descriptions	Edit	Release Date
0.1	Preliminary New release	Gong huimei	2024-01-03

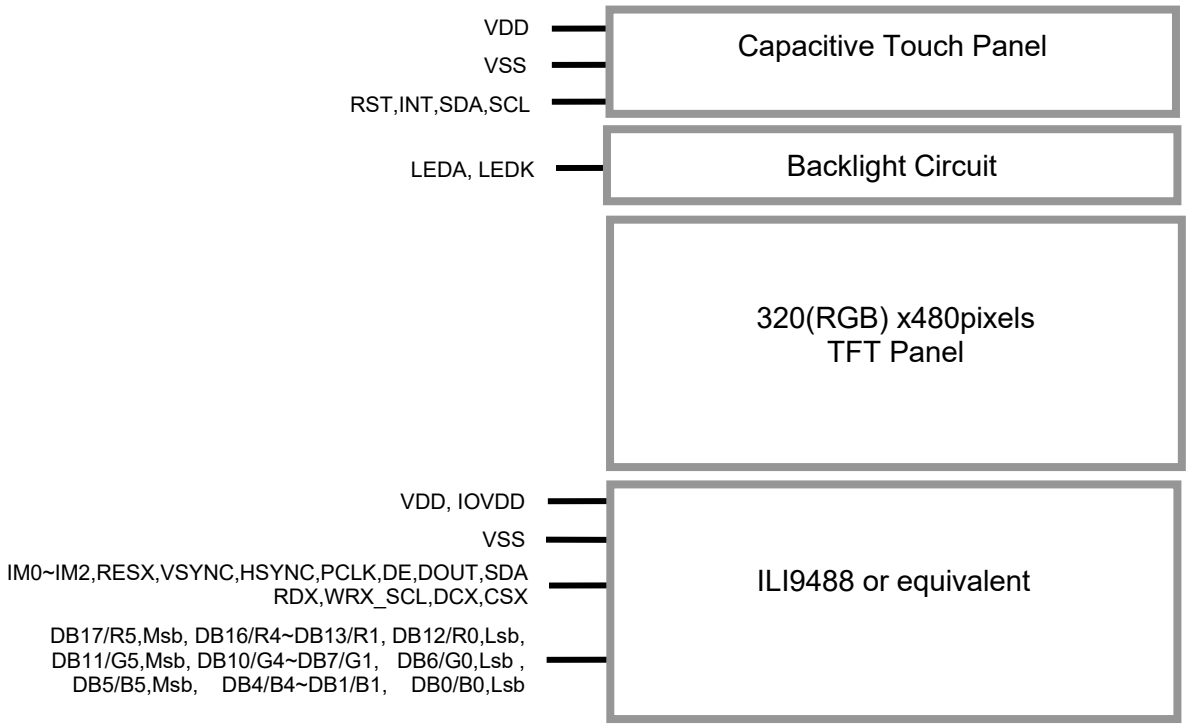
Table of Content

1. General Specifications

Screen Size(Diagonal) :	3.5”
Active Area :	48.96x73.44mm
Number of dots :	320(RGB)x480
Pixel Pitch :	0.153x0.153mm
Color Depth:	262k Colors
Display Technology :	a-Si TFT active matrix
Display Mode :	Normally White,Transmissive
Display Interface :	MCU/RGB+SPI
Viewing Direction :	12H (*1) (gray scale inverse) 6H (*2)
Touch Panel :	Capacitive Touch Panel
Surface Treatment:	Glare
Touch Interface:	IIC Touch Interface
Storage Temperature :	-30 ~ +80°C
Operating Temperature :	-20 ~ +70°C

Note:
*1. For saturated color display content (eg. pure-red, pure-green, pure-blue or pure-colors-combinations).
*2. For “color scales” display content.
*3. Color tone may slightly change by temperature and driving condition.

1.1 Block Diagram



2. Terminal Functions

2.1 TFT Interface Terminal

Pin No.	PIN Name	I/O	Descriptions
1	VSS	P	Negative power supply,0V
2,3	IOVDD	P	I/O Positive Power
4,5	VDD	P	Positive power supply
6	IM0	I	MPU system interface mode select
7	IM1	I	MPU system interface mode select
8	IM2	I	MPU system interface mode select
9	RESX	I	Reset signal RESX = L, Initialization is executed RESX = H, Normal running
10	VSYNC	I	Vertical sync, signal in RGB mode If no used, please connect this pin to VSS
11	HSYNC	I	Horizontal sync, signal in RGB mode If no used, please connect this pin to VSS
12	PCLK	I	Pixel clock signal in RGB mode If no used, please connect this pin to VSS
13	DE	O	Data enable signal in RGB mode If no used, please connect this pin to VSS
14	DB17/R5,Msb	I/O	Data Bus
15	DB16/R4	I/O	
:	:	:	
18	DB13/R1	I/O	
19	DB12/R0,Lsb	I/O	
20	DB11/G5,Msb	I/O	
21	DB10/G4	I/O	
:	:	:	
24	DB7/G1	I/O	
25	DB6/G0,Lsb	I/O	
26	DB5/B5,Msb	I/O	
27	DB4/B4	I/O	
:	:	:	
30	DB1/B1	I/O	
31	DB0/B0,Lsb	I/O	
32	VSS	P	Negative power supply,0V
33	DOUT	O	Serial data output pin If no used, leave this pin open
34	SDA	I/O	Serial data input /output bi-direction pin If no used, please connect this pin to VSS
35	RDX	I	Serve as a read signal If no used, please connect this pin to IOVDD
36	WRX_SCL	I	(WR) Write data enable pin in DBI Type B (SCL) Write data enable pin in DBI Type C If no used, please connect this pin to IOVDD
37	DCX	I	Data/Command Selection pin Low: Command High: Parameter If no used, please connect this pin to IOVDD
38	CSX	I	Chip select signal If no used, please connect this pin to IOVDD
39	NC(XR)	-	No connect
40	NC(YD)		
41	NC(XL)		
42	NC(YU)		
43	LEDA	P	LED ANODE
44~49	LEDK	P	LED CATHODE
50	VSS	P	Negative power supply,0V

Note1:I--Input，O--Output，P--Power/Ground,VDD=VDD
Note2:If use the RGB interface,need to initialize the interface with 3/4-Line SPI before using RGB to transfer data

IM2	IM1	IM0	Interface	WR/SCL	DATA Bus use	
					Command/Parament	GRAM
0	0	0	DBITYPE-B18-bit (DB_EN='0')	WR	DB7~DB0	DB17 ~DB0:18bits Data
0	0	1	DBI TYPE-B 9-bit	WR	DB7~DB0	DB8 ~DB0: 9bits Data
0	1	0	DBI TYPE-B 16-bit	WR	DB7~DB0	DB15~DB0:16bits Data
0	1	1	DBI TYPE-B 8-bit	WR	DB7~DB0	DB7 -DB0:8bits Data
1	0	1	DBI TYPE-C Option 1(3 wire)	SCL	SDA/DOUT	
1	1	1	DBI TYPE-C Option 3(4 wire)	SCL	SDA/DOUT	

System interface select

2.2 CTP Interface Terminal

Pin No.	PIN Name	I/O	Descriptions
1	RST	I	Reset Pin
2	VDD	P	Voltage power
3	GND	P	Ground
4	INT	O	External interrupt to the host
5	SDA	I/O	IIC data input and output
6	SCL	I	IIC clock input

Note:The capacitance touch drive IC is GT911,Please refer to IC: GT911 data sheet for more details.

3. Absolute Maximum Ratings

Items	Symbol	Min.	Max.	Unit	Condition
Power Voltage	VDD	-0.3	+3.3	V	V_{SS} = 0V
Input Voltage	V_{IN}	-0.3	+3.3	V	V_{SS} = 0V
Operating Temperature	T_{OP}	-20	+70	°C	No Condensation
Storage Temperature	T_{ST}	-30	+80	°C	No Condensation

Cautions:
Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

4. Electrical Characteristics

4.1 DC Characteristics of TFT LCD Panel

V_{SS}=0V, T_{OP}=25°C

Items		Symbol	MIN.	TYP.	MAX.	Unit	Condition / Application Pin
Operating Voltage		VDD	2.5	2.8	3.3	V	VDD,IOVDD
Input Signal Voltage	High Level	V_{IH}	0.7xV_{DD}	-	V_{DD}	V	IM0~IM2,RESX,VSYNC,HSYNC, PCLK,DB17~DB0,SDA,RDX, WRX_SCL,DCX,CSX
	Low Level	V_{IL}	-0.3	-	0.3xV_{DD}	V	
Output Low Voltage	High Level	V_{OH}	0.8xV_{DD}		V_{DD}	V	DB17~DB0,DE,SDA,DOUT
	Low Level	V_{OL}	0	-	0.2xV_{DD}	V	
Operating Current		I_{DD}	-	12	-	mA	VDD (*1)

Note: *1. VDD=2.8V

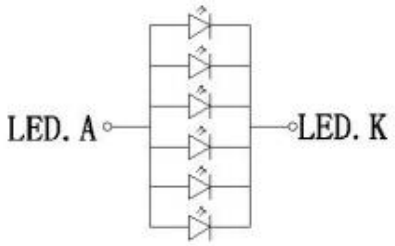
4.2 DC Characteristics of CTP

Items	Symbol	MIN.	TYP.	MAX.	Unit	Condition / Application Pin
Operating Voltage	VDD	2.8	-	3.3	V	VDD,IOVDD
Operating Current	I_{DD}	-	8	14.5	mA	VDD active current
Operating Temperature	T_{OP}	-40	25	85	°C	
Storage Temperature	T_{ST}	-60	25	125	°C	

4.3 LED Backlight Circuit Characteristics

T_{OP} =25°C

Items	Symbol	MIN.	TYP.	MAX.	Unit	Remark
Forward Voltage	Vf	2.7	3.2	3.4	V	For each LED
Forward Current	If	-	120	-	mA	For total LED
LED lifetime	-	-	30000	-	Hours	



CIRCUIT DIAGRAM

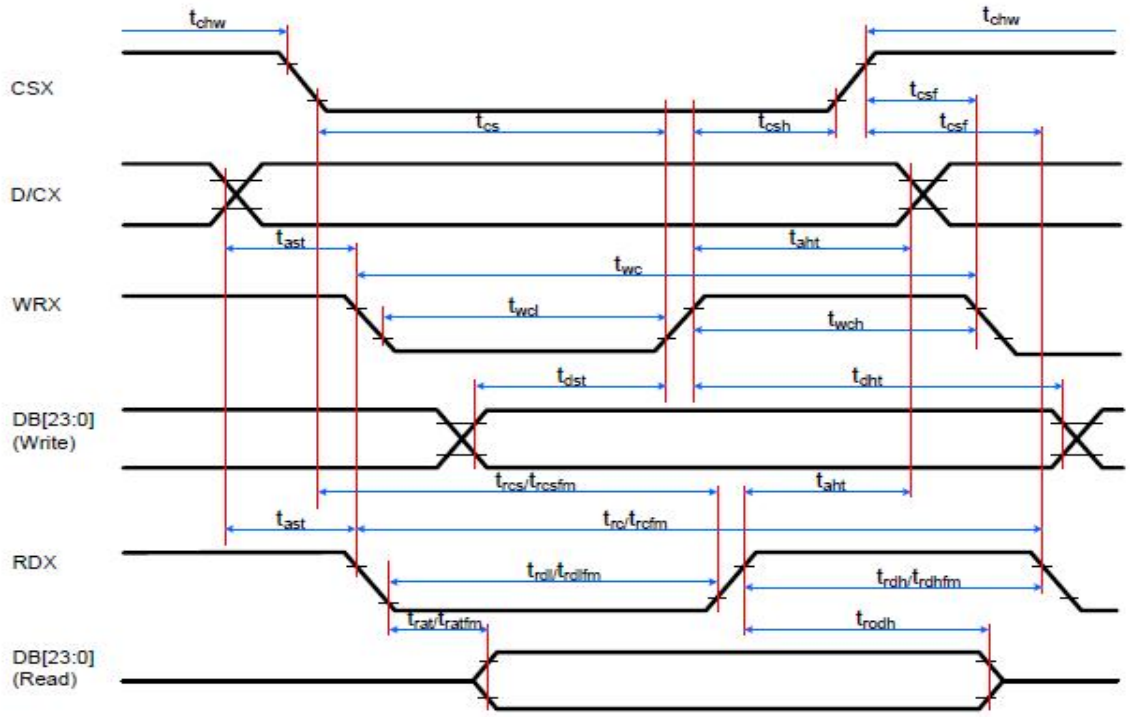
If=120mA/Vf=3.2V (TYP)

Note1: The LED driving condition is defined for each LED module (1LED Serial, 6LED Parallel).
Note2: Under LCM operating, the stable forward current should be inputted. And forward voltage is for reference only.
Note3: Optical performance should be evaluated at Ta=25℃ only If LED is driven by high current, high ambient temperature & humidity condition. The life time of LED will be reduced. Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.At the same time the luminance of Backlight would decrease under the hight temperature.
Note4: The LED driving condition is defined for each LED module.

5. AC Characteristics

5.1 DBI Type B

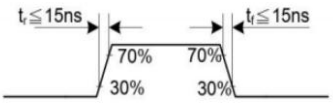
5.1.1 DBI Type B Timing Characteristic



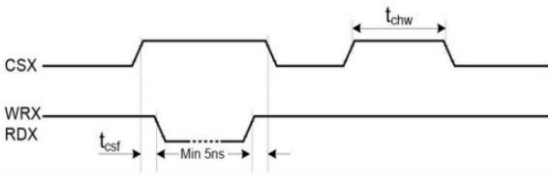
Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	-
	taht	Address hold time (Write/Read)	0	-	ns	-
CSX	tchw	CSX "H" pulse width	0	-	ns	-
	tcs	Chip Select setup time (Write)	15	-	ns	-
	trcs	Chip Select setup time (Read ID)	45	-	ns	-
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	-
	tcsf	Chip Select Wait time (Write/Read)	0	-	ns	-
WRX	twc	Write cycle	40	-	ns	-
	twrh	Write Control pulse H duration	15	-	ns	-
	twrl	Write Control pulse L duration	15	-	ns	-
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	When read from Frame Memory
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	When read ID data
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
DB [23:0], DB [17:0], DB [15:0], DB [8:0], DB [7:0]	tdst	Write data setup time	10	-	ns	For maximum, CL=30pF For minimum, CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Notes:

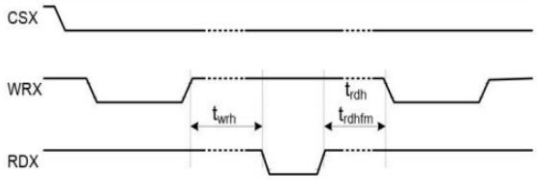
1. Ta = -30 to 70 °C, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, VSS=0V
2. Logic high and low levels are specified as 30% and 70% of IOVCC for input signals.
3. Input signal rising time and falling time:



4. The CSX timing:



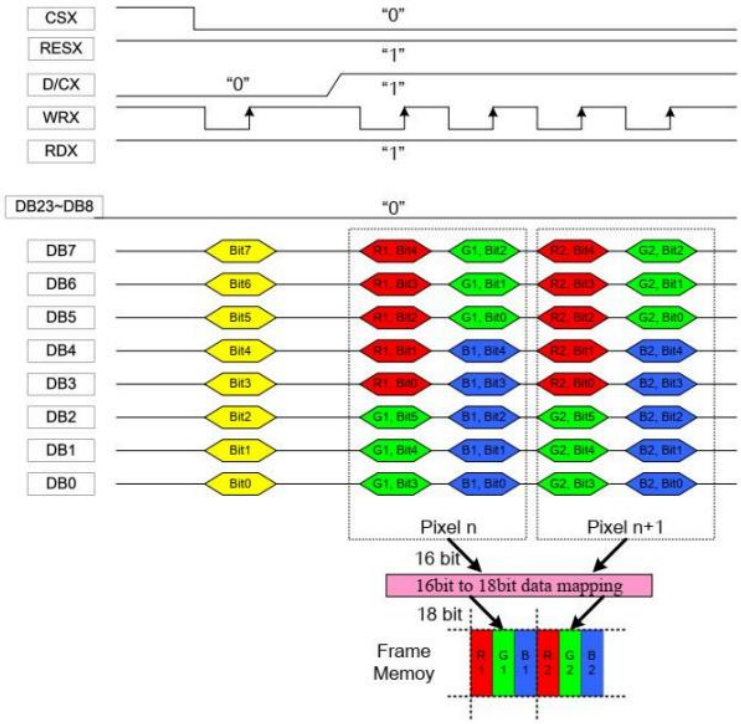
5. The Write to Read or the Read to Write timing:



Please refer to IC: ILI9488 data sheet for more details.

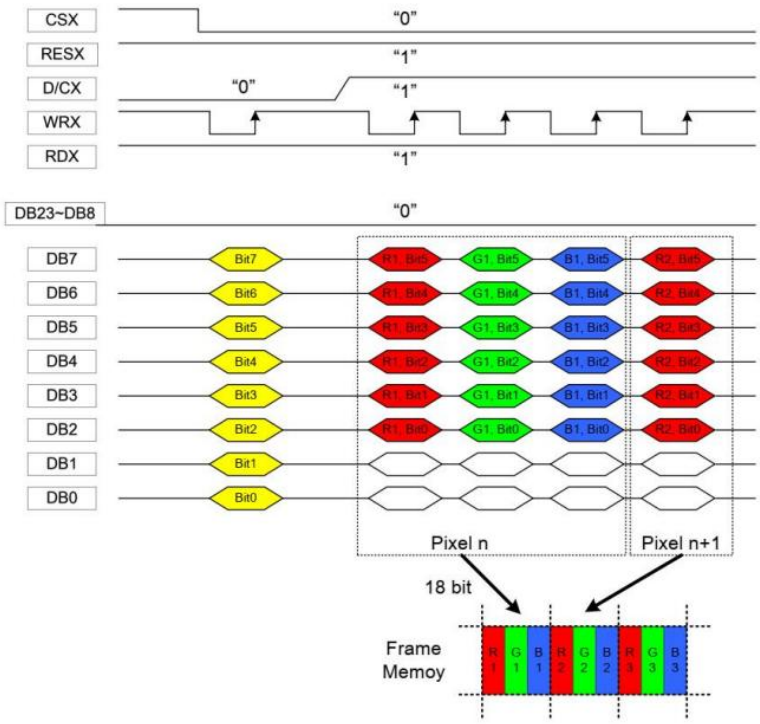
5.1.2 DBI Type B Data Bus

8-bit Data Bus for 16-bit/pixel (RGB 5-6-5 Bits Input), 65K-color



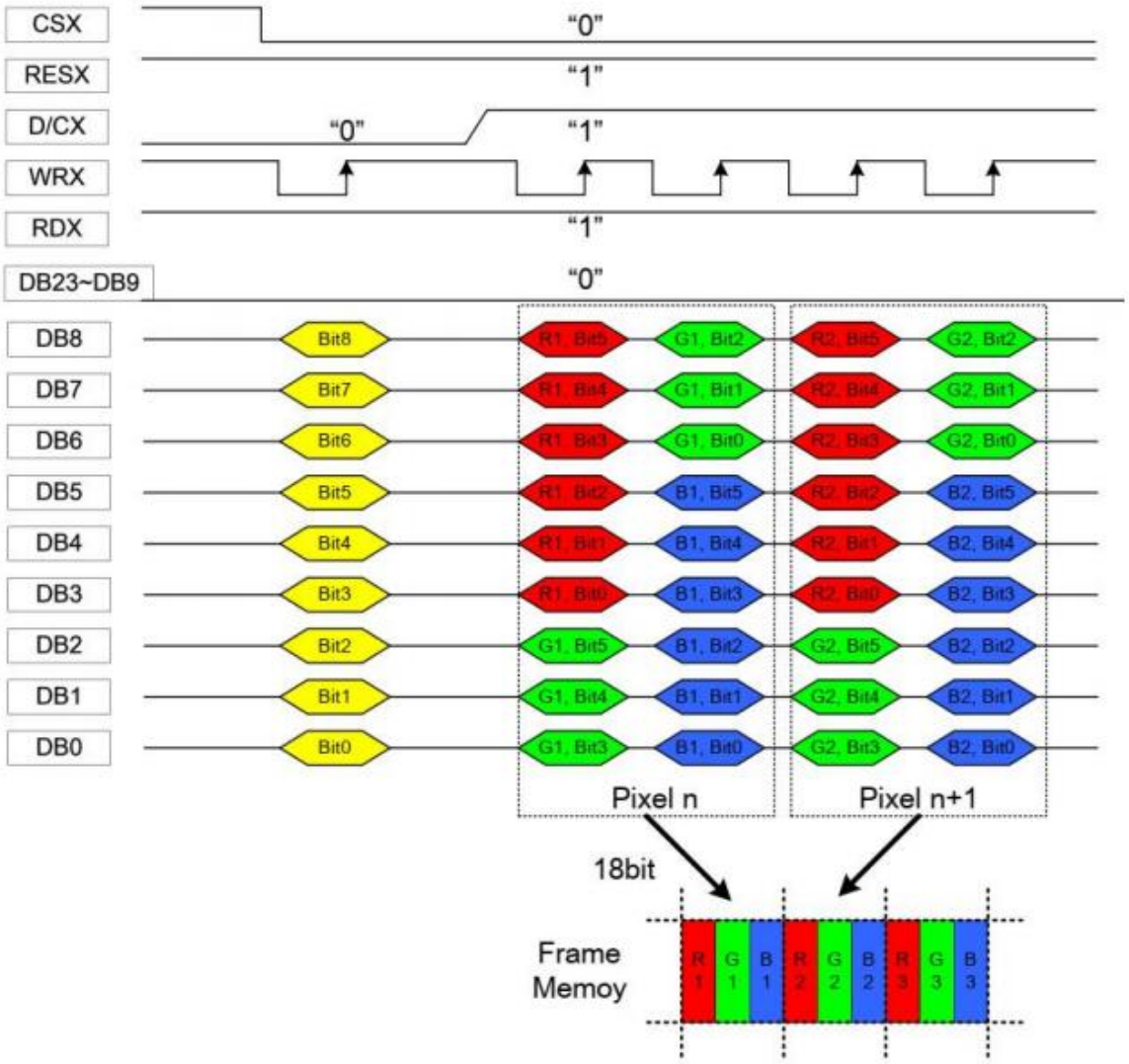
Notes:
1. The data order is as follows: MSB = DB7, LSB =DB0, and picture data is MSB = Bit 5, LSB= Bit 0 for Green data, and MSB = Bit 4, LSB = Bit 0 for Red and Blue data.
2. 2-times transfer is used to transmit 1 pixel data to the 16-bit color depth information.
3.'-'= void

8-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color



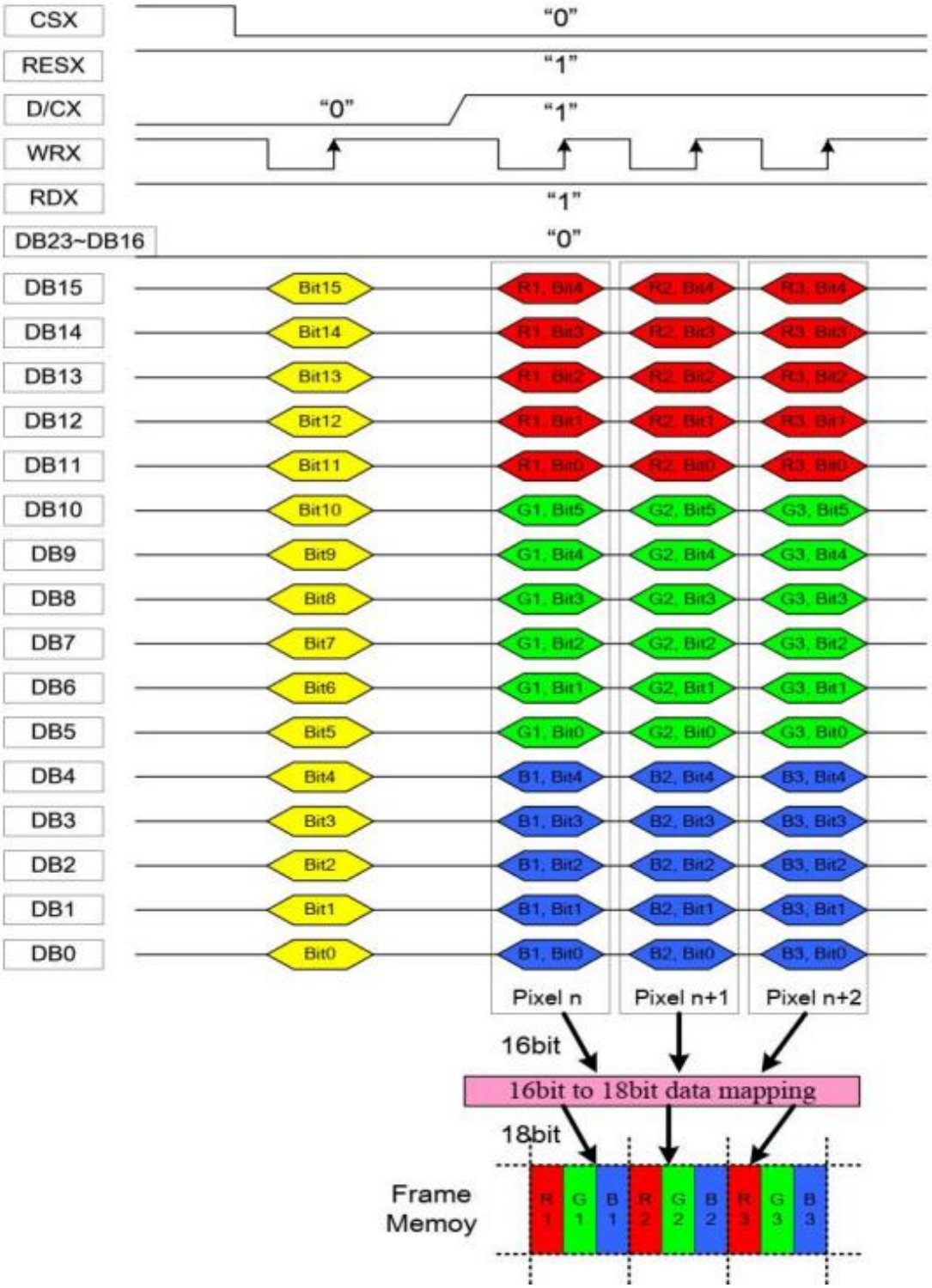
Notes:
1. The data order is as follows: MSB = DB7, LSB =DB0, and picture data is MSB = Bit 5, LSB= Bit 0 for Green data, and MSB = Bit 4, LSB = Bit 0 for Red and Blue data.
2. 3-times transfer is used to transmit 1 pixel data to the 18-bit color depth information.
3.'-'= void

9-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color



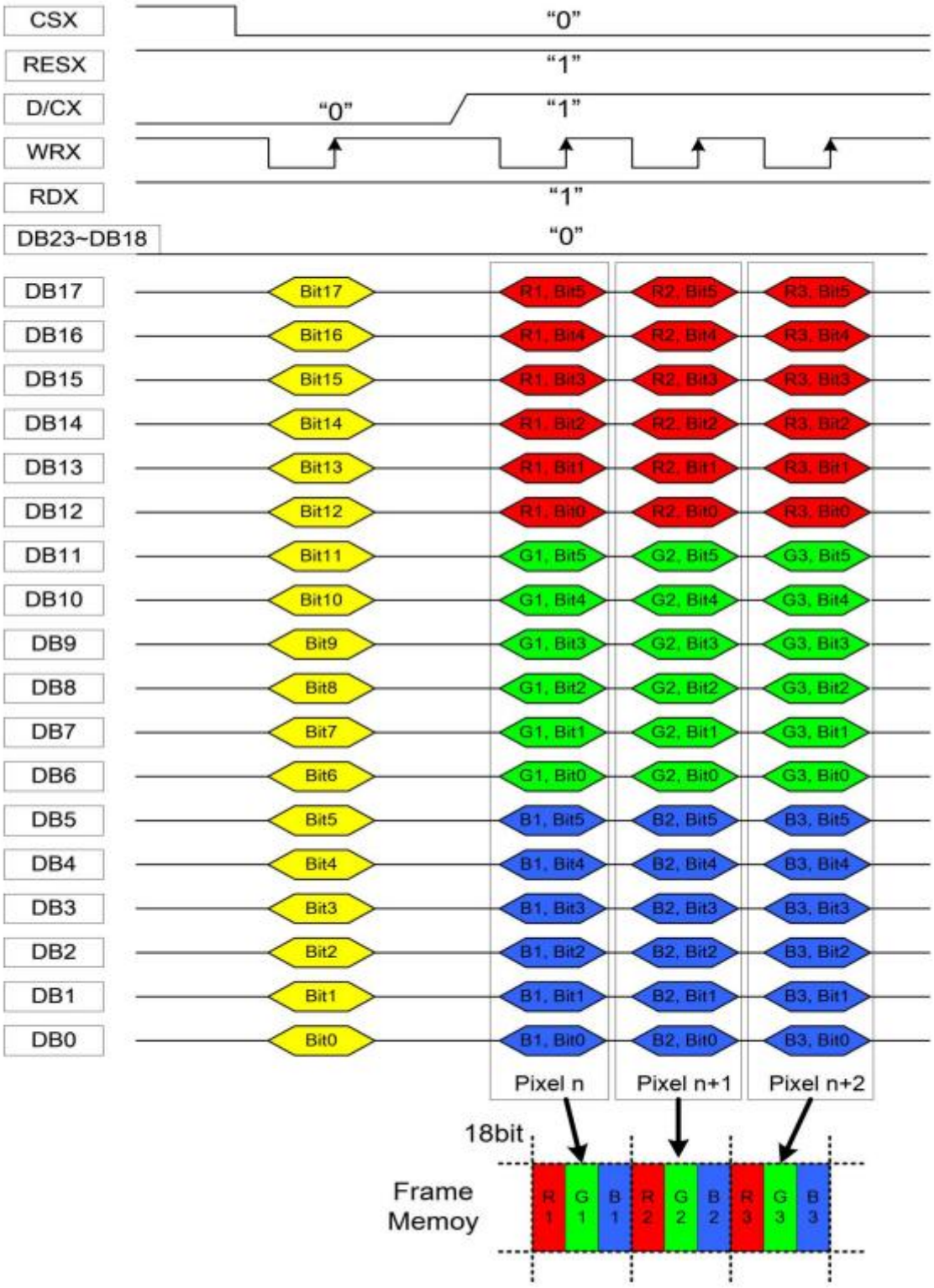
Notes:
1. The data order is as follows: MSB = DB8, LSB =DB0, and picture data is MSB = Bit 5, LSB= Bit 0 for Green, Red and Blue data.
2. 2-times transfer is used to transmit 1 pixel data to the 18-bit color depth information.
3.'-'= void

16-bit Data Bus for 16-bit/pixel (RGB 5-6-5 Bits Input), 65K-color



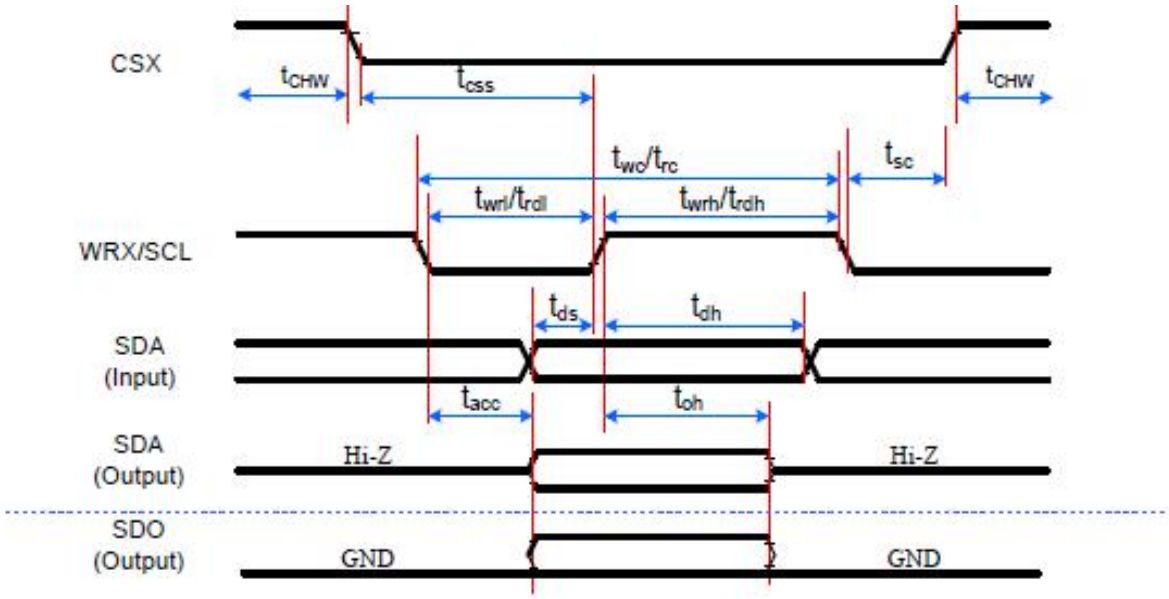
Notes:
1. The data order is as follows: MSB = DB15, LSB =DB0, and picture data is MSB = Bit 5, LSB= Bit0 for Green data, and MSB = Bit4, LSB =Bit0 for Red and Blue data.
2. 1-times transfer is used to transmit 1 pixel data to the 16-bit color depth information.
3.'-'= void

18-bit Data Bus for 18-bit/pixel (RGB 6-6-6 Bits Input), 262K-color



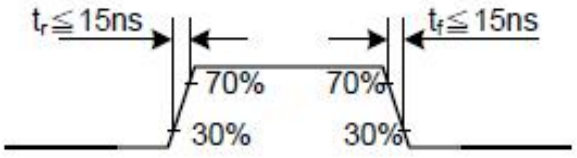
Notes:
1. The data order is as follows: MSB = DB17, LSB =DB0, and picture data is MSB = Bit 5, LSB= Bit0 for Green , Red and Blue data.
2. 1-times transfer is used to transmit 1 pixel data to the 18-bit color depth information.

5.2 3-Line SPI Interface Timing Characteristic



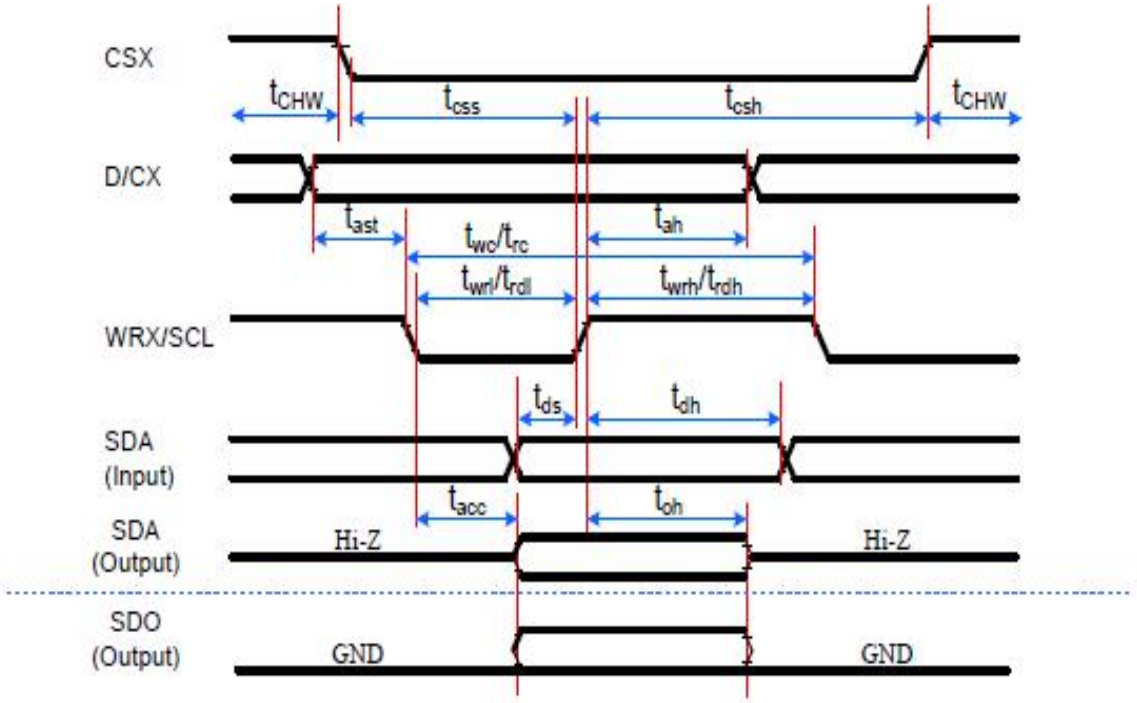
Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tsc	SCL-CSX	15	-	ns	
	tchw	CSX H Pulse Width	40	-	ns	
	tcss	Chip select time (Write)	60	-	ns	
	tcsh	Chip select hold time (Read)	65	-	ns	
SCL	twc	Serial Clock Cycle (Write)	66	-	ns	
	twrh	SCL H Pulse Width (Write)	15	-	ns	
	twrl	SCL L Pulse Width (Write)	15	-	ns	
	trc	Serial Clock Cycle (Read)	150	-	ns	
	trdh	SCL H Pulse Width (Read)	60	-	ns	
	trdl	SCL L Pulse Width (Read)	60	-	ns	
SDA (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF
	toh	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Note: Ta = -30 to 70 °C, IOVDD,VDD=2.5V to 3.3V,VSS=0V, T = 10+/-0.5ns



Please refer to IC: ILI9488 data sheet for more details.

5.3 4-Line SPI Interface Timing Characteristic

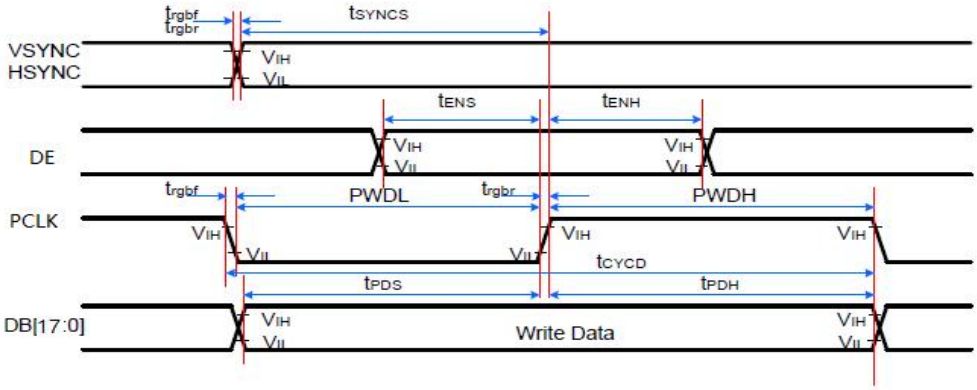


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	15	-	ns	
	tcsh	Chip select hold time (Read)	15	-	ns	
	tCHW	CS H pulse width	40	-	ns	
SCL	twc	Serial clock cycle (Write)	50	-	ns	
	twrh	SCL H pulse width (Write)	10	-	ns	
	twrl	SCL L pulse width (Write)	10	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL H pulse width (Read)	60	-	ns	
	trdl	SCL L pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-	ns	
	tah	D/CX hold time (Write/Read)	10	-	ns	
SDA (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF
	tod	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Note1:Ta=-30 to 70℃，IOVDD，VDD=2.5V to 3.3V，VSS=0V，T=10+/-0.5ns.
Note2:Does not include signal rising and falling times.
Please refer to IC: ILI9488 data sheet for more details.

5.4 DPI Interface

5.4.1 DPI Interface Characteristic



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/ HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	16-/18-/24-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
DB[17:0]	t_{PDS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
PCLK	PWDH	DOTCLK high-level period	20	-	ns	
	PWDL	DOTCLK low-level period	20	-	ns	
	t_{CYCD}	DOTCLK cycle time	50	-	ns	
	t_{rgbr}, t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, IOVCC , VDD=2.5V to 3.3V, VSS=0V, T=10+/-0.5ns.

Please refer to IC: ILI9488 data sheet for more details.

5.4.2 DPI Interface pixel format

18-bit DPI interface connection (DB [17:0] is used): set pixel format DPI [2:0] = 3'h6

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
						R[5]	R4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

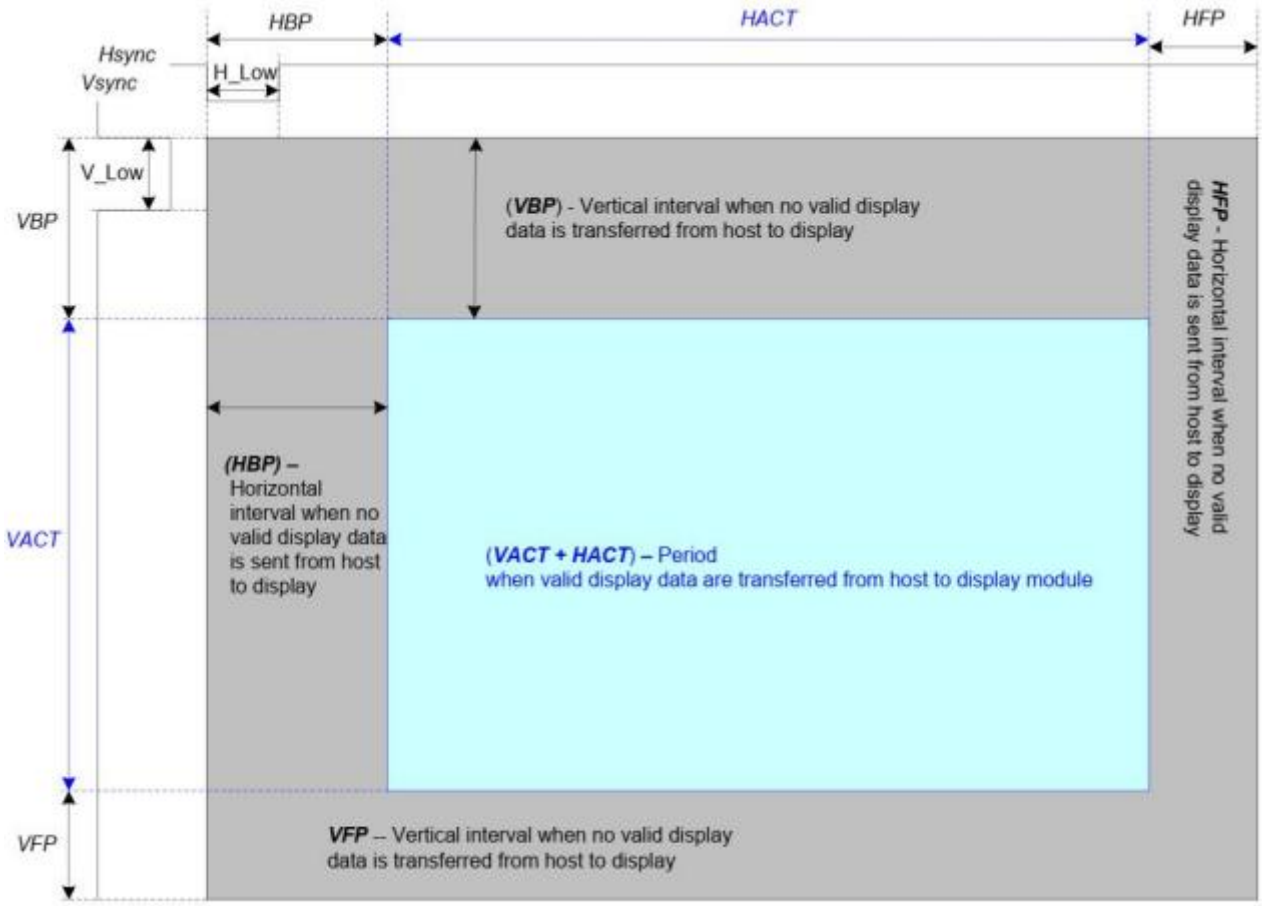
16-bit DPI interface connection (DB [15:0] is used): set pixel format DPI [2:0] = 3'h5

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
								R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

The Pixel clock (DCLK) runs all the time without stop. It is used to enter VS, HS, DE and D[17: 0] states when there is a rising edge of the DCLK. The DCLK cannot be used as the internal clock for other functions of the display module.
Vertical synchronization (VS) is used to indicate when a new frame of the display is received. This is low enable and its state is read to the display module by a rising edge of the DCLK signal.
Horizontal synchronization (HS) IS used to indicate when a new line of the frame is received. This is low enable and its state is read to the display module by a rising edge of the DCLK signal.
Data Enable (DE) is used to indicate when the RGB information that should be transferred in the display is received. This is a high enable, and its state is read to the display module by a rising edge of the DCLK signal.
D[17:0] is used to indicate what is the information of the image that is transferred on the display (when DE = 0 (low) and there is a rising edge of DCLK). D[17:0] can be 0(low) or 1(high). These lines are read by a rising edge of the DCLK signal. In RGB interface modes, the input display data is written to GRAM first then outputs the corresponding source voltage according to the gray data from GRAM.

Note：Please refer to IC: ILI9488 data sheet for more details.

5.4.3 DPI(RGB) Interface timing



DPI Parameters Setting(BYPASS bit = 0)

Parameters	Symbols	Min.	Typ.	Max.	Units
Horizontal Synchronization	H_Low	3	-	H_Low < HBP	DOTCLK
Horizontal Back Porch	HBP	3	-	192	DOTCLK
Horizontal Front Porch	HFP	3	-	255	DOTCLK
Horizontal Address	HACT	-	320	-	DOTCLK
Horizontal Frequency		-	-	33	KHz
Vertical Synchronization	V_Low	1	-	V_Low < VBP	Line
Vertical Back Porch	VBP	2	-	V_Low+VBP+VFP < 32	Line
Vertical Front Porch	VFP	2	-		Line
Vertical Address	VACT	-	480	-	Line
Vertical Frequency		60	-	70	Hz
DOTCLK cycle		100	-	50	ns
DOTCLK Frequency		10	-	20	MHz

DPI Parameters Setting(BYPASS bit = 1)

Parameters	Symbols	Min.	Typ.	Max.	Units
Horizontal Synchronization	H_Low	3	-	H_Low < HBP	DOTCLK
Horizontal Back Porch	HBP	20	-	192	DOTCLK
Horizontal Front Porch	HFP	70	-	255	DOTCLK
Horizontal Address	HACT	-	320	-	DOTCLK
Horizontal Frequency		-	-	33	KHz
Vertical Synchronization	V_Low	1	-	V_Low < VBP	Line
Vertical Back Porch	VBP	2	-	V_Low+VBP+VFP < 32	Line
Vertical Front Porch	VFP	2	-		Line
Vertical Address	VACT	-	480	-	Line
Vertical Frequency		60	-	70	Hz
DOTCLK cycle		83.3	-	50	ns
DOTCLK Frequency		12	-	20	MHz

$$\text{Frame Rate} = \frac{\text{DOTCLK}}{(\text{Display Pixel}+\text{HBP}+\text{HFP}) \times (\text{Display line}+\text{VBP}+\text{VFP})}$$

Display line : The number of gate-lines

Display pixel :The number of pixels in one gate-line

Example：DOTCLK = 20Mhz, TE=70Hz, VBP=2, VFP=2, HBP=100, HFP=170.

Note: VBP[4:0]/HBP[7:0] (Blanking Porch Control, RB5h) define as follows:

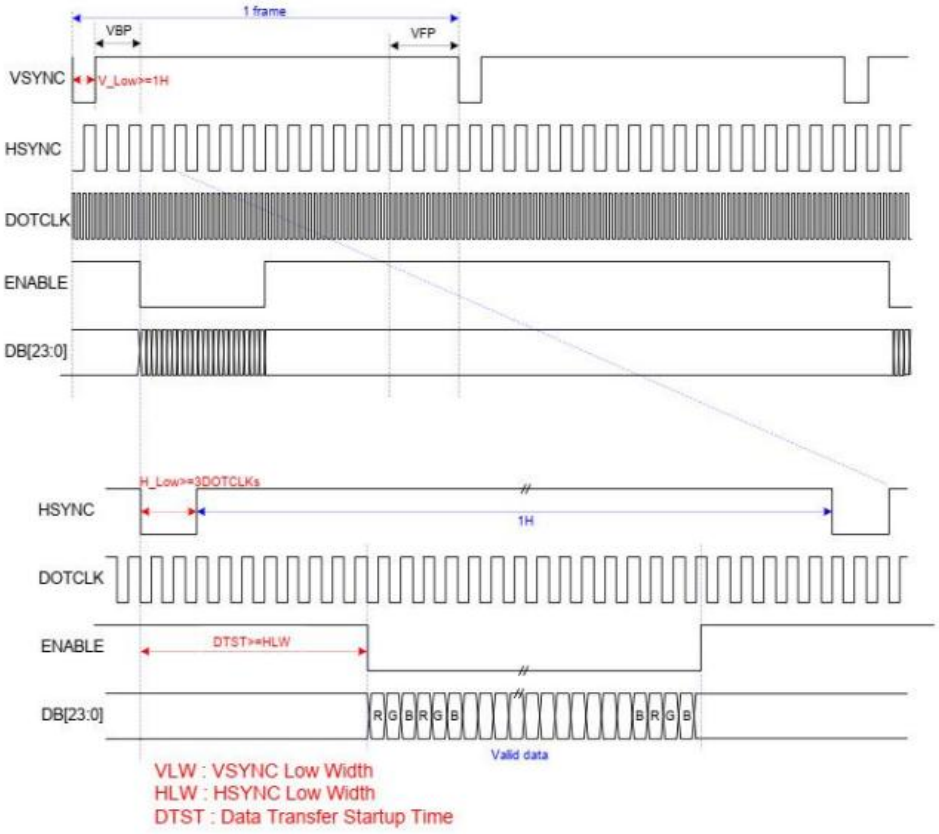
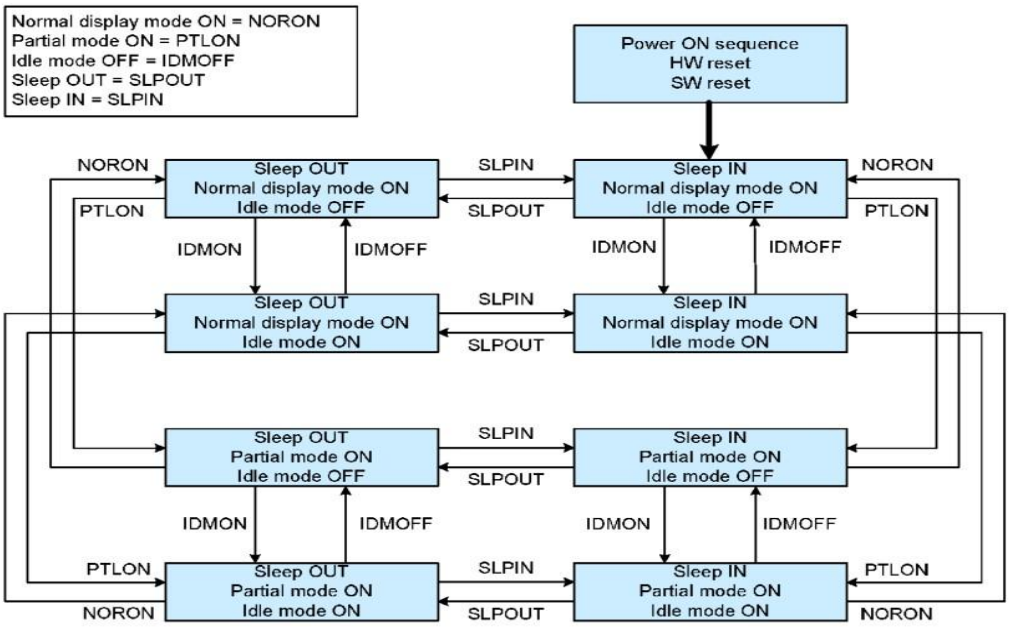


Figure 19: DPI Interface Timing Diagram

Note: VSPL = 0, HSPL = 0, DPL = 0 and EPL = 0 of Interface Mode Control B0h command.

5.5 Power ON/OFF Sequence



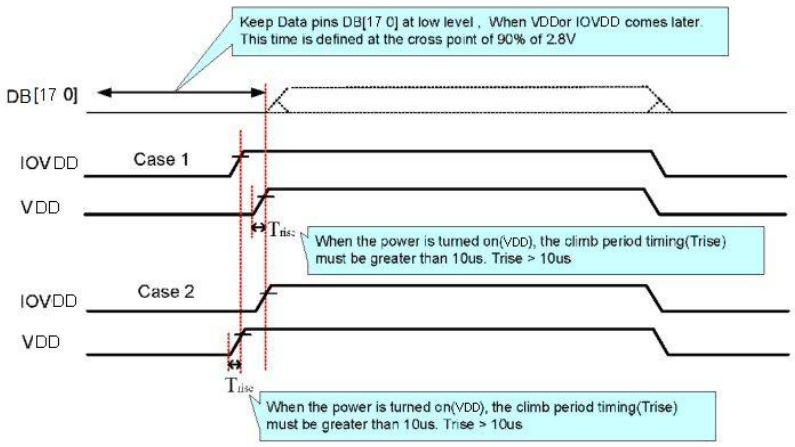
Notes:

1. There are not any abnormal visual effects when one power mode changes to another power mode.
2. There is not any limitation, which is not specified by users, when one power mode changes to another power mode.

IOVDD and VDD can be applied or powered down in any order. During the Power Off sequence ,if the LCD is in the Sleep In mode, VDD and IOVDD must be powered down with a minimum of 120 msec.If the LCD is in the Sleep In mode, VDD and IOVDD can be powered down with a minimum of 0msec after the /RST has been released. /CS can be applied at any time or can be permanently grounded. /RST has priority over /CS.

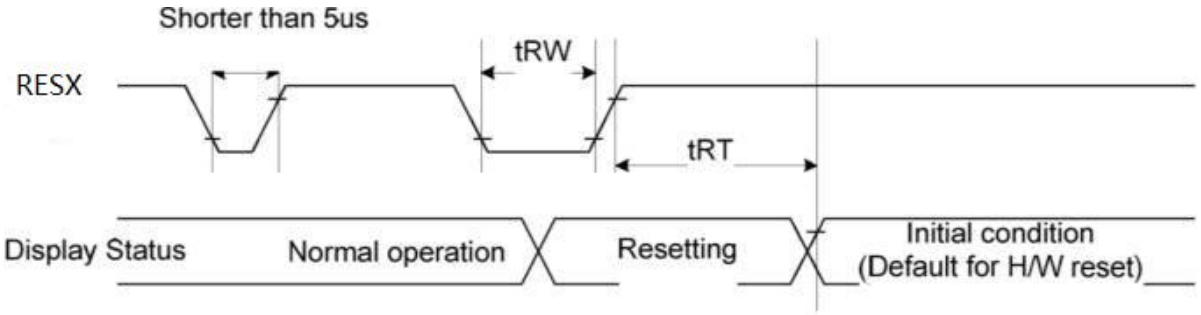
Notes:

1. There will be no damage to the ILI9488 if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequence.
3. There will be no abnormal visible effects on the display between the end of the Power On Sequence and before receiving the Sleep Out command, and also between receiving the Sleep In command and the Power Off Sequence.
4. If the /RST line is not steadily held by the host during the Power On Sequence as defined in Sections 11.1 and 11.2 (ILI9488 datasheet), then it will be necessary to apply the Hardware /RST after the completion of the Host Power On Sequence to ensure correct operations. Otherwise, all the functions are not guaranteed.
5. When the power is turned on, the climb period timing (Trise) must be greater than 10us.
6. Keep data pins D[17:0] at low level, or IOVDD comes later



Note：Please refer to IC: ILI9488 data sheet for more details.

5.6 Reset timing



Item	Symbol	MIN.	TYP.	MAX.	Unit
Reset LOW pulse width	t_{RW}	1.0	-	-	us
Reset time	T_{RT}	-	-	120	ms

Please refer to IC: ILI9488 data sheet for more details.

6 . Optical Characteristics

T_{OP} =25°C

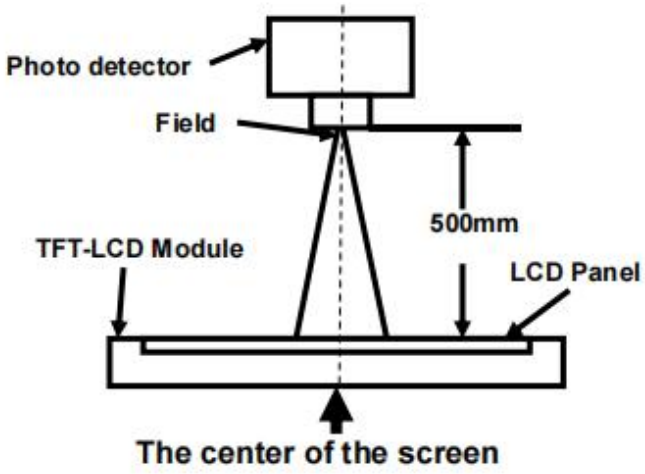
Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles		θT	CR≧10	-	70	-	Degree	Note2,3
		θB		-	60	-		
		θL		-	70	-		
		θR		-	70	-		
Contrast Ratio		CR	θ= 0°	350	500	-	-	Note 3
Response Time		T_{ON}	25℃	-	25	-	ms	Note 4
		T_{OFF}						
Chromaticity	White	x	Backlight is on	0.236	0.286	0.336	-	Note 1,5
		y		0.266	0.316	0.366		
	Red	x		0.586	0.636	0.686		
		y		0.284	0.334	0.384		
	Green	x		0.276	0.326	0.376		
		y		0.543	0.593	0.643		
	Blue	x		0.100	0.150	0.200		
		y		0.027	0.077	0.127		
Uniformity		U		80	-	-	%	Note 6
NTSC		S	Θ= 0° Φ=0°	60	-	-	%	Note 5
Luminance		L		250	300	-	cd/㎡	Note 7

Note：

IF= 120mA, and the ambient temperature is 25℃

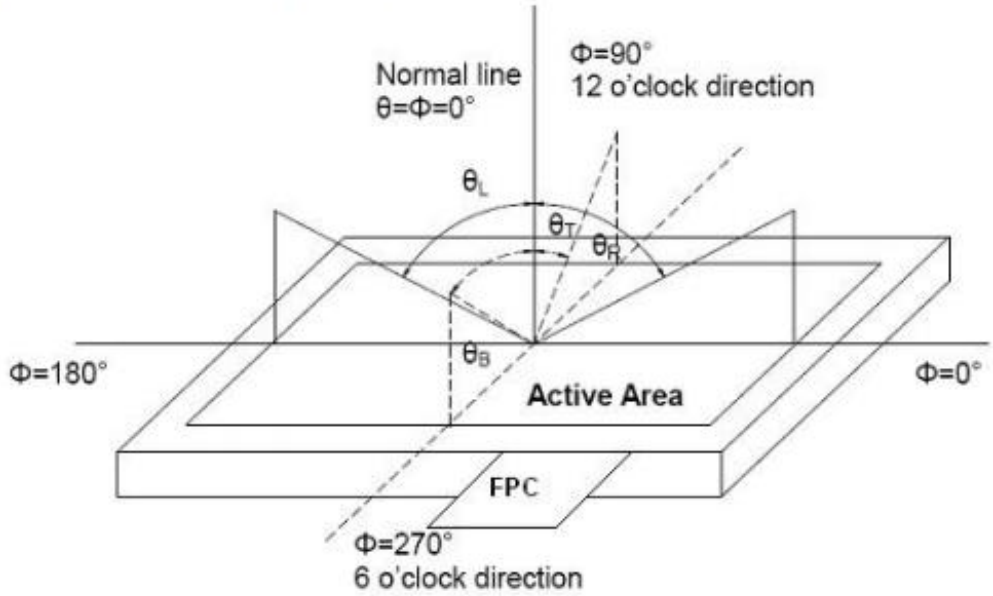
Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 Minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Note 2: Definition of viewing angle range and measurement system.

viewing angle is measured at the center point of the LCD。



Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

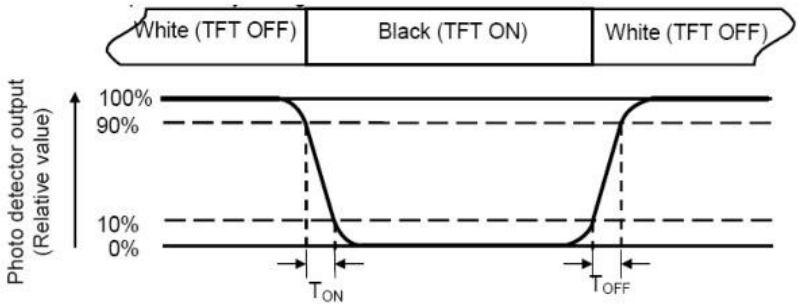
"White state ": The state is that the LCD should drive by Vwhite.

"Black state": The state is that the LCD should drive by Vblack.

Vwhite: TBD V Vblack: TBD V.

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

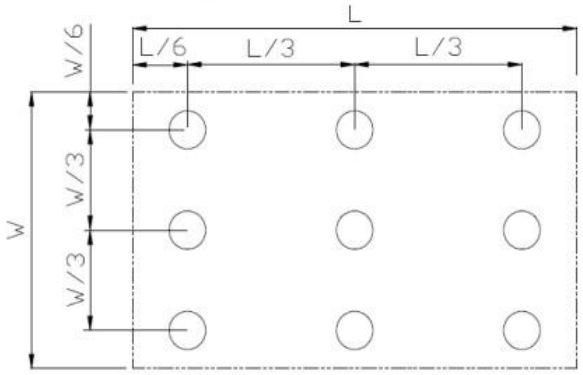
Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/ Lmax

L-------Active area length W----- Active area width



Lmax: The measured Maximum luminance of all measurement position.

Lmin: The measured Minimum luminance of all measurement position.

Note 7: Definition of Luminance:

Measure the luminance of white state at center point.

7 . LCD Module Design and Handling Precautions

- Please ensure V0, VCOM is adjustable, to enable LCD module get the best contrast ratio under different temperatures, view angles and positions.
- Normally display quality should be judged under the best contrast ratio within viewable area. Unexpected display pattern may com out under abnormal contrast ratio.
- Never operate the LCD module exceed the absolute maximum ratings.
- Never apply signal to the LCD module without power supply.
- Keep signal line as short as possible to reduce external noise interference.
- IC chip (e.g. TAB or COG) is sensitive to light. Strong light might cause malfunction. Light sealing structure casing is recommended.
- Make sure there is enough space (with cushion) between case and LCD panel, to prevent external force passed on to the panel; otherwise that may cause damage to the LCD and degrade its display result.
- Avoid showing a display pattern on screen for a long time (continuous ON segment).
- LCD module reliability may be reduced by temperature shock.
- When storing and operating LCD module, avoids exposure to direct sunlight, high humidity, high or low temperature. They may damage or degrade the LCD module.
- Never leave LCD module in extreme condition (max./min storage/operate temperature) for more than 48hr.
- Recommend LCD module storage conditions is 0 C~40 C <80%RH.
- LCD module should be stored in the room without acid, alkali and harmful gas.
- Avoid dropping & violent shocking during transportation, and no excessive pressure press, moisture and sunlight.
- LCD module can be easily damaged by static electricity. Please maintain an optimum anti-static working environment to protect the LCD module. (eg. ground the soldering irons properly)
- Be sure to ground the body when handling LCD module.
- Only hold LCD module by its sides. Never hold LCD module by applying force on the heat seal or TAB.
- When soldering, control the temperature and duration avoid damaging the backlight guide or diffuser which might degrade the display result such as uneven display.
- Never let LCD module contact with corrosive liquids, which might cause damage to the backlight guide or the electric circuit of LCD module.
- Only clean LCD with a soft dry cloth, Isopropyl Alcohol or Ethyl Alcohol. Other solvents (e.g. water) may damage the LCD.
- Never add force to components of LCD module. It may cause invisible damage or degrade the module's

7. 液晶显示模块设计和使用须知

- 请注意 VO, VCOM 的设定，以确保液晶显示模块在不同的使用温度下以及在不同的视角和位置观察模块显示，均能达到最佳对比度，请务必将应用电路上设置为对比度可调。
- 请注意液晶显示模块的显示品质判定是指在正常对比度下以及视窗(V.A)范围内进行的，非正常对比度下液晶可能会出现非预期的显示不良，应注意区分。
- 请勿在最大额定值以外使用液晶显示模块。
- 请勿在没有接通电源的条件下，给液晶显示模块输送信号。
- 请尽可能缩短信号线的连接，以避免对液晶显示模块的信号干扰。
- 集成电路因 IC 芯片(如 TAB 或 COG)对紫外线极为敏感，强光环境下可能会引起液晶显示模块功能失效，故应采用不透光的外壳。
- 请在液晶显示模块与外壳之间保留足够的空间(可使用衬垫)，以缓冲外力对液晶显示模块的损坏或因受力不均而产生的显示不匀等异常现象。
- 避免液晶显示屏在某一画面下长时间点亮，否则有出现残影的风险；请通过软件每隔一段时间改变一次画面。
- 液晶显示模块的可靠性可能因温度冲击而降低。
- 请勿在阳光直射、高湿、高温或低温下储存和使用液晶显示模块，这将造成液晶显示模块的损坏或失效。
- 请勿在极限环境(最大/最小存储/工作温度)下使用或放置液晶显示模块超过 48 小时以上。
- 液晶显示模块建议存储条件为：0 C~40 C <80%RH。
- 请勿让液晶显示模块存储于带有 酸性，碱性，有害气体环境之中。
- 在运输过程中，请勿让液晶显示模块跌落与猛烈震动，同时避免 异常挤压，高湿度，与阳光照射.
- 液晶显示模块极易受静电损坏，请务必保证液晶显示模块在防静电的工作环境中使用或保存。(如：烙铁正确接地,等)
- 拿取液晶显示模块时需注意操作人员的接地情况。
- 请手持液晶显示模块的边沿取放模块，防止热压纸或 TAB 部位受力。
- 焊接液晶模块时，请注意控制烙铁的温度、焊接时间，以免烫坏导光板或偏光片，导致显示不匀等不良现象发生。
- 请勿使用洗板水等腐蚀性液体接触液晶模块，以免腐蚀导光板或模块电路。
- 仅可使用柔软的干布，异丙醇或乙醇清洁液晶屏表面，其他任何溶剂(如:水)都有可能损坏液晶模块。
- 请勿挤压液晶显示模块上的元器件，以避免产生潜在的损坏或失效而影响产品可靠性。

reliability.
- When mounting LCD module, please make sure it is free from twisting, warping and bending.
- Do not add excessive force on surface of LCD, which may cause the display color change abnormally.
- LCD panel is made with glass. Any mechanical shock (e.g. dropping from high place) will damage the LCD module.
- Protective film is attached on LCD screen. Be careful when peeling off this protective film, since static electricity may be generated.
- Polarizer on LCD gets scratched easily. If possible, do not remove LCD protective film until the last step of installation.
- When peeling off protective film from LCD, static charge may cause abnormal display pattern. The symptom is normal, and it will turn back to normal in a short while.
- LCD panel has sharp edges, please handle with care.
- Never attempt to disassemble or rework LCD module.
- If display panel is damaged and liquid crystal substance leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes promptly wash it off using soap and water.

- 装配液晶显示模块时，请务必注意避免液晶显示模块的扭曲或变形。
- 请勿挤压液晶显示屏表面，这将导致显示颜色的异常。
- 液晶屏由玻璃制作而成，任何机械碰撞(如从高处跌落)均有可能损坏液晶显示模块。
- 液晶屏表面带有保护膜，揭除保护膜时需要注意可能产生的静电。
- 因液晶显示屏表面的偏光片极易划伤，安装完成之前请尽量不要揭下保护膜。
- 请缓慢揭除保护膜，在此过程中液晶显示屏上可能会产生静电线，此为正常情况，可在短时间内消失。
- 请注意避免被液晶显示屏的边缘割伤。
- 请不要试图拆卸或改造液晶显示模块。
- 当液晶显示屏出现破裂，内部液晶液体可能流出；相关液体不可吞吃，绝对不可接触嘴巴，如接触到皮肤或衣服，请使用肥皂与清水彻底清洗.

8 . CTP Mounting Instructions

8. 电容触摸屏安装指导

8.1 Surface Mounting (Figure 2)
- As the CTP assembling on the countersink area with double side adhesive.
  The countersink area should be flat and clean to ensure the double side adhesive installation result.
- The Bezel is recommend to keep a gap (≥0.3mm each side) around the cover lens for tolerance.
- It is recommended to provide an additional support bracket with gasket for backside support when necessary (e.g. TFT module without mounding structure). They should only provide appropriate support and keep the module in place.
- The mounting structure should be strong enough to prevent external uneven force or twist act onto the module

8.1 嵌入安装（附图 2）
- 客户面框应具有使用双面胶粘贴 CTP 的结构沉台面，其粘贴面要求平整且洁净无污以保证粘贴牢靠.
- 考虑到制作误差，建议面框与 CTP 盖板之间四周留有≥0.3㎜ 间隙.
- 建议必要时在背面提供垫有胶垫附加支架(例如无安装结构的 TFT 模块)，应仅利用适当支撑以保持模块位置.
- 安装结构应具有足够的强度，以防止外部不均匀力或扭曲力作用到模块上。

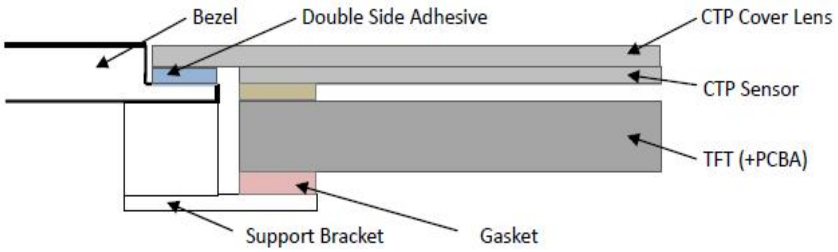


Figure 2

8.2 Additional Cover Lens Mounting (Figure 3)
- For the case of additional cover Lens mounting, it is necessary to recheck with the CTP specification about the material and thickness to ensure the functionality.
- It should keep a 0.2~0.3mm gap between the cover lens and the CTP surface..
- The cover lens window should be bigger than the active area of the CTP.It should be≥0.5mm each side.
- It is recommended to provide an additional support

8.2 覆加盖板（附图 3）
- 需要覆加玻璃盖板的安装，为确保其功能，有必要查看产品规格书中有关盖板材料和厚度的说明.
- 玻璃盖板与 CTP 表面之间应留有 0.2～0.3㎜ 间隙.
- 玻璃盖板视窗应大于 CTP 动作区域，各边离动作区应≥0.5㎜。
- 建议必要时在背面提供附加支架(例如无安装结构的

bracket for backside support when necessary (e.g. slim type TFT module without mounding structure). They should only provide appropriate support and keep the module in place.

- The mounting structure should be strong enough to prevent external uneven force or twist act onto the module.

薄型 TFT 模块)，应仅利用适当支撑以保持模块位置.

- 安装结构应具有足够的强度，以防止外部不均匀力或扭曲力作用到模块上.

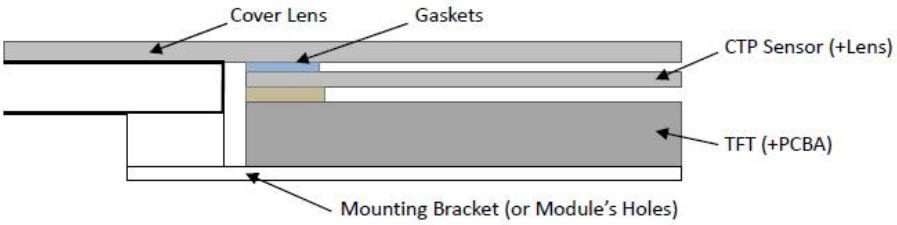
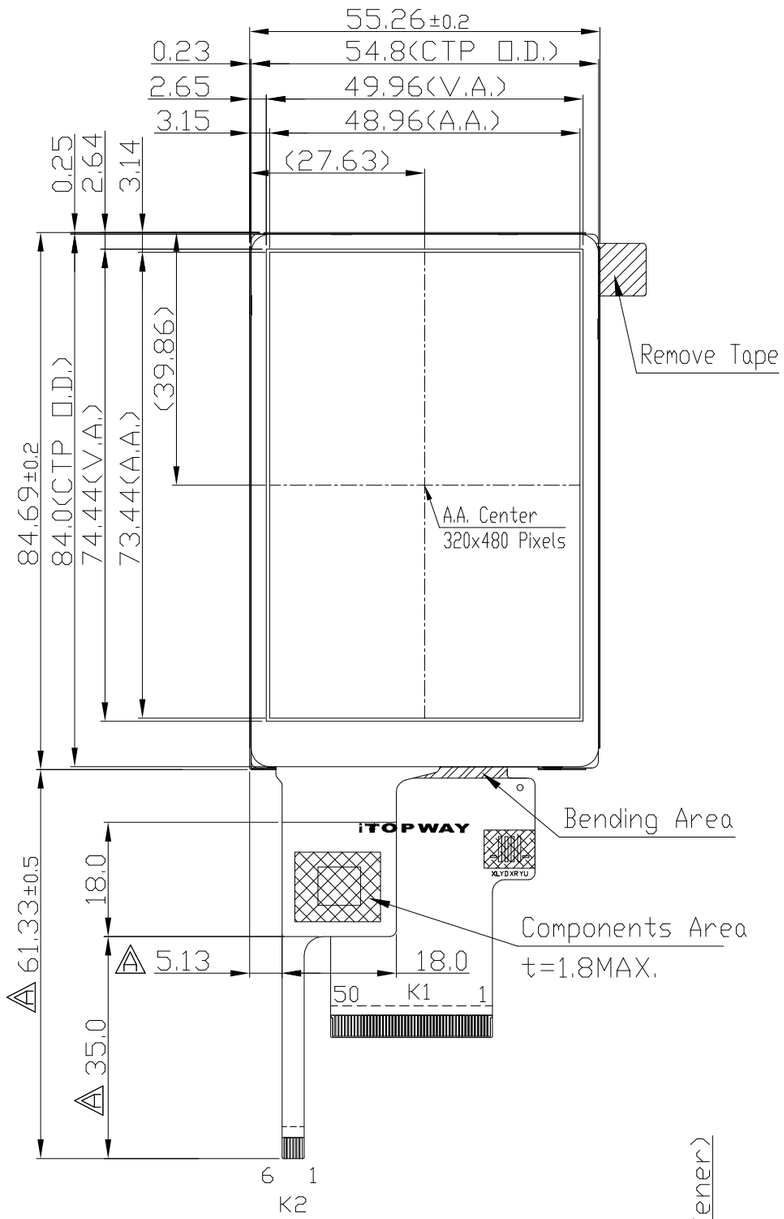


Figure 3

Warranty

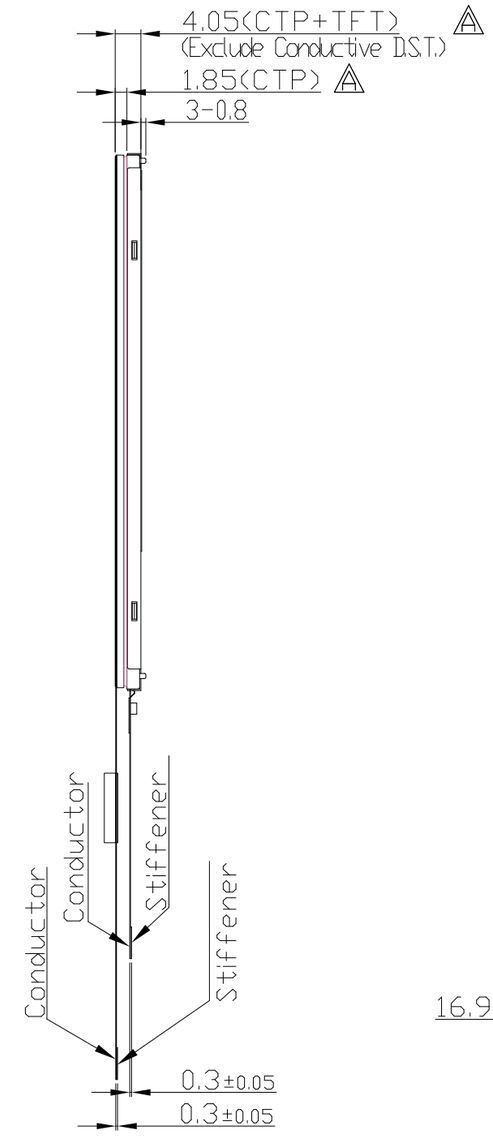
This product has been manufactured to our company's specifications as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we cannot take responsibility if the product is used in medical devices, nuclear power control equipment, aerospace equipment, fire and security systems, or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required. If the product is to be used in any of the above applications, we will need to enter into a separate product liability agreement.

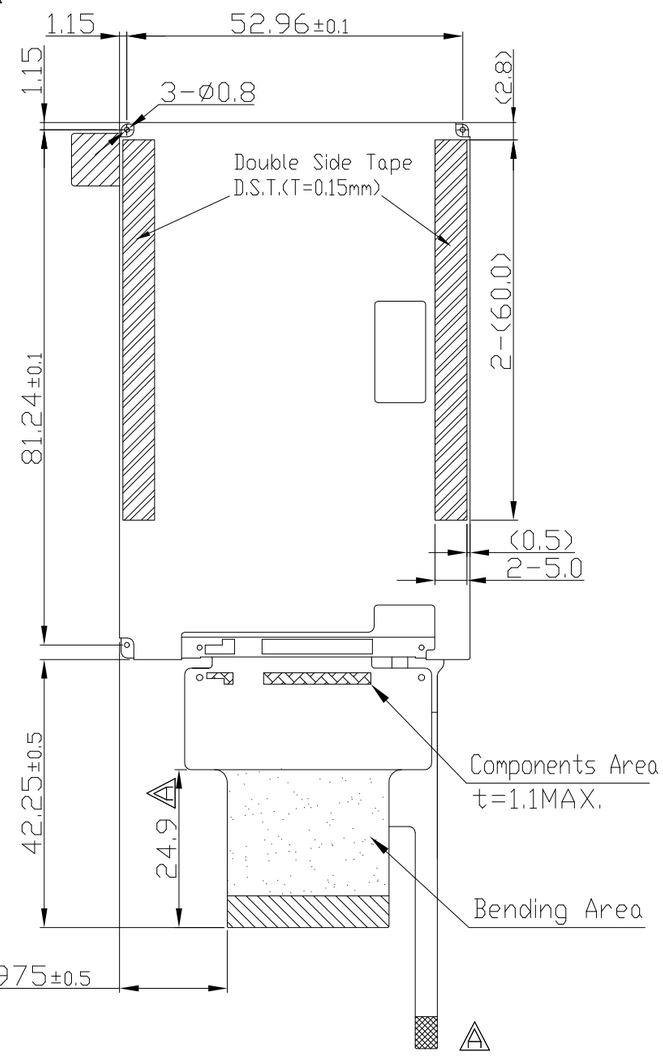
- We cannot accept responsibility for any defect, which may arise form additional manufacturing of the product (including disassembly and reassembly), after product delivery.
- We cannot accept responsibility for any defect, which may arise after the application of strong external force to the product.
- We cannot accept responsibility for any defect, which may arise due to the application of static electricity after the product has passed our company's acceptance inspection procedures.
- When the product is in CCFL models, CCFL service life and brightness will vary according to the performance of the inverter used, leaks, etc. We cannot accept responsibility for product performance, reliability, or defect, which may arise.
- We cannot accept responsibility for intellectual property of a third part, which may arise through the application of our product to our assembly with exception to those issues relating directly to the structure or method of manufacturing of our product.

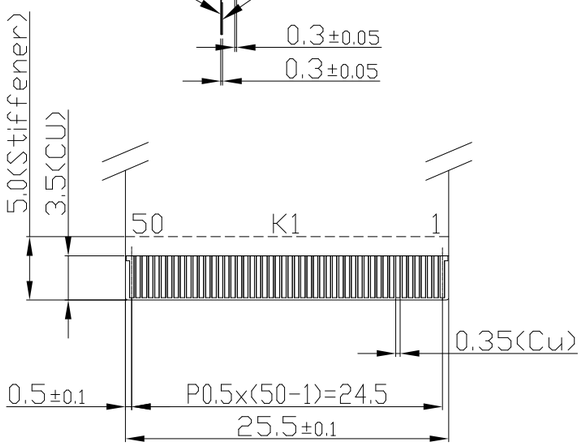


Note:

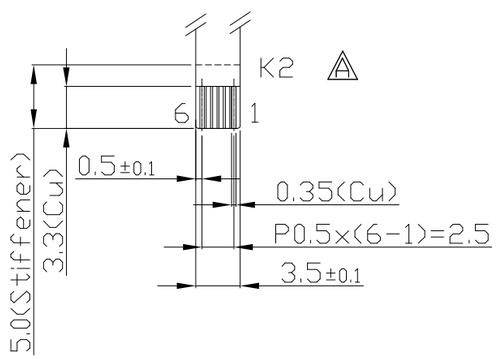
*1. LCD Display Type : TFT,Transmissive
*2. Pixel Arrangment : RGB-STRIPE
*3. Color Depth : 262k Color
*4. □perating Voltage(VDD , IO□VDD) : 2.8V
*5. Backlight : White LEDs
*6. Backlight Supply : 6x20mA (VF=3.2V, TYP)
*7. Matched Connector :
K1 FH19SC-50S-0.5SH(HIR□S) □r Equivalent
K2 Molex 54550-0633 or equivalent
*8. CTP Driver IC : GT911
*9. □perating Temperature : -20°C~70°C
*10. Storage Temperature : -30°C~80°C
*11. Unmarked Tolerace : ≤150,±0.3; >150,±0.5







K1 Details
Scale 2/1



K2 Details
Scale 2/1

K1 Terminal	
No.	Pin Name
1	VSS
2	IO□VDD
3	IO□VDD
4	VDD
5	VDD
6	IM0
7	IM1
8	IM2
9	RESX
10	VSYNC
11	HSYNC
12	PCLK
13	DE
14	DB17/R5,Msb
15	DB16/R4
16	DB15/R3
17	DB14/R2
18	DB13/R1
19	DB12/R0,Lsb
20	DB11/G5,Msb
21	DB10/G4
22	DB9/G3
23	DB8/G2
24	DB7/G1
25	DB6/G0,Lsb

K1 Terminal	
No.	Pin Name
26	DB5/B5,Msb
27	DB4/B4
28	DB3/B3
29	DB2/B2
30	DB1/B1
31	DB0/B0,Lsb
32	VSS
33	DO□UT
34	SDA
35	RDX
36	WRX_SCL
37	DCX
38	CSX
39	NC(XR)
40	NC(YD)
41	NC(XL)
42	NC(YU)
43	LEDA
44	LEDK
45	LEDK
46	LEDK
47	LEDK
48	LEDK
49	LEDK
50	VSS

K2 Terminal	
No.	Pin Name
1	RST
2	VDD
3	GND
4	INT
5	SDA
6	SCL

B		
A	Revise □utline	2023-11-29 Taoqingwen
Rev	Note	Date

Dwg Title: LMT035DNJFWD-NND □utline Dwg

Dwg No.: MK-008222a-1-1 | Date: 2023-11-14

Scale: 1/1 | Tol. | Unit: mm | Paper Size: A3

Approved | Checked | Drawn: Tao qingwen

TOPWAY